CS401- Computer Architecture and Assembly Language

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□1 argument
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□1 argument
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□3 arguments
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□No arguments

Question No: 2 (M - 1) .

In STOSB instruction SI is decremented or incremented by

4

1

2

3

Question No: 3 (M - 1) .

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CMPS instruction subtracts the source location to the destination location.

Destination location always lies in

DS:SI

DS:DI

ES:SI

ES:DI

Question No: 4 (M - 1) .

Regarding assembler, which statement is true:

Assembler converts mnemonics to the corresponding OPCODE

Assembler converts OPCODE to the corresponding mnemonics.

Assembler executes the assembly code all at once

Assembler executes the assembly code step by step

Question No: 5 (M - 1) .

Iof “BB” is the OPCODE of the instruction which states to “move a constant value to AX register”, the hexadecimal representation (Using little Endian notation) of the instruction “Mov AX,336” (“150” in hexadecimal number system) will be:

0xBB0150

0x5001BB

0x01BB50

0xBB5001

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Question No: 6 (M - 1) .

In the instruction MOV AX, 5 the number of operands are

1

2

3

4

Question No: 7 (M - 1) .

The maximum parameters a subroutine can receive (with the help of registers) are

6

7

8

9

Question No: 8 (M - 1) .

In assembly the CX register is used normally as a _____register.

source

counter

index

pointer

Question No: 9 (M - 1) .

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All the addressing mechanisms in iAPX 8 8 return a number called _ _ _ _ _ _ _ _ _ _ _ _ _ _ address .

effective

faulty

indirect

direct

Question No: 10 (M - 1) .

When a 16 bit number is divided by an 8 bit number, the dividend will be in

AX

BX

CX

DX

Question No: 11 (M - 1) .

in Left-Shift-Operation the left most bit _____

will drop

will go into CF

Will come to the right most

will be always 1

Question No: 12 (M - 1) .

Suppose the decimal number "35" after shifting its binary two bits to left, the new value becomes _____

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35

70

140

17

Question No: 13 (M - 1) .

When divide overflow occurs processor will be interrupted this type of interrupt is called

Hardware interrupt

Software interrupt

Processor exception

Logical interrupts

Question No: 14 (M - 1) .

Which mathematical operation is dominant during the execution of SCAS instruction

Division

Multiplication

Addition

Subtraction

Question No: 15 (M - 1) .

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After the execution of REP instruction CX will be decremented then which of the following flags will be affected?

CF

OF

DF

No flags will be affected

Question No: 16 (M - 1) .

_____ is one of the reasons due to which string instructions are used in 8088

Efficiency and accuracy

Reduction in code size and accuracy

Reduction in code size and speed

Reduction in code size and efficiency

Question No: 17 (M - 1)

Write any two control instructions.

Question No: 18 (M - 1)

RET instruction take how many arguments

Question No: 19 (M - 2)

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Explain the fuction of rotate right (ROR) instruction

Question No: 20 (M - 2)

Describe the PUSH function

Question No: 21 (M - 3)

Write down the names of four segment registers?

Question No: 22 (M - 3)

For what purpose "INT 4" is reserved?

Question No: 23 (M - 5)

Given that [BX+0x0100] BX=0x0100
Ds=0xFFF0
Calculate the physical address

Question No: 1 (M - 1) .

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Th

e physical address of the stack is obtained by

► **SS:SP combination**

► SS:SI combination

► **SS:SP combination**

► ES:BP combination

► ES:SP combination

Question No: 2 (M - 1) .

Aft

er the execution of instruction “RET ”

► **SP is incremented by 2**

► **SP is incremented by 2**

► SP is decremented by 2

► SP is incremented by 1

► SP is decremented by 1

Question No: 3 (M - 1) .

Th

e second byte in the word designated for one screen location holds

► **Character color on the screen**

► The dimensions of the screen

► Character position on the screen

► **Character color on the screen**

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► ASCII code of the character

Question No: 4 (M - 1) .

RE

P will always

► **Decrement CX by 1**

► Increment CX by 1

► Increment CX by 2

► **Decrement CX by 1**

► Decrement CX by 2

Question No: 5 (M - 1) .

Th

e basic function of SCAS instruction is to

► **Compare**

► **Compare**

► Scan

► Sort

► Move data

Question No: 6 (M - 1) .

Ind

ex registers are used to store _____

► **Address**

► Data

► Intermediate result

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► **Address**

► Both data and addresses

Question No: 7 (M - 1) .

Th

e bits of the _____ work independently and individually

► **flags register**

► index register

► base register

► **flags register**

► accumulator

Question No: 8 (M - 1) .

To

convert any digit to its ASCII representation

► **Add 0x30 in the digit**

► **Add 0x30 in the digit**

► Subtract 0x30 from the digit

► Add 0x61 in the digit

► Subtract 0x61 from the digit

Question No: 9 (M - 1) .

W

hen a 32 bit number is divided by a 16 bit number, the quotient is of

► **4 bits**

► 32 bits

► 16 bits

► 8 bits

► **4 bits**

Question No: 10 (M - 1) .

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W

hen a 16 bit number is divided by an 8 bit number, the quotient will be in

► **AL**

► AX

► **AL**

► AH

► DX

Question No: 11 (M - 1) .

W

hich mathematical operation is dominant during the execution of SCAS instruction

► **Division**

► **Division**

► Multiplication

► Addition

► Subtraction

Question No: 12 (M - 1) .

If

AX contains decimal -2 and BX contains decimal 2 then after the execution of instructions:

CMP AX, BX

JA label

► **Zero flag will set**

► Jump will be taken

► **Zero flag will set**

► ZF will contain value -4

► Jump will not be taken

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Question No: 13 (M - 1) .

The execution of the instruction “mov word [ES : 160], 0x1230” will print a character “0” on the screen at

► **First column of second row**

► Second column of first row

► **First column of second row**

► Second column of second row

► First column of third row

Question No: 14 (M - 1) .

If the direction of the processing of a string is from higher addresses towards lower addresses then

► **DF is cleared**

► ZF is cleared

► **DF is cleared**

► ZF is set

► DF is set

Question No: 15 (M - 1) .

The instruction ADC has_____ Operand(s)

► **3**

► 0

► 1

► 2

► **3**

Question No: 16 (M - 1) .

Which bit of the attributes byte represents the red component of background color ?

► **3**

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► **3**

► 4

► 5

► 6

Question No: 17 (M - 2)

What is difference between SHR and SAR instructions?

SHR

The SHR inserts a zero from the left and moves every bit one position to the right and copy the rightmost bit in the carry flag.

SAR

The SAR shift every bit one place to the right with a copy of the most significant bit left at the most significant place. The bit dropped from the right is caught in the carry basket. The sign bit is retained in this operation.

Question No: 18 (M - 2)

For what purpose "**INT 1**" is reserved ?

Question No: 19 (M - 2)

Define implied operand?

It is always in a particular register say the accumulator. It needs to not be mentioned in the instruction.

Q=1:

Which bit of attributes byte represents the blue component of foreground color?

- 0
- 1
- 2
- 3

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Q=2:

The clear screen operation initializes the whole block of video memory to:

- 0417
- 0714
- 0741
- 017

Q=3:

When the operand of DIV instruction is of 16 bit then implied dividend will be of

- 64-bit
- 32-bits
- 16-bits
- 8--bits

Q=4

Which of the following is the pair of register used to access memory instring instruction:

- DI and BP
- SI and BP
- DI and SI
- DS and Si

Q=5

A fat32 file system directory entry in DOS consist of how many bytes?

- 16
- 24
- 32
- 64

Q=6:

Which register is generally used to specify the services number of an interrupt?

DX

AX

BX

CX

……

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Q=7:

In 9 pin db 9 connector ,which pin is assigned to RD(received data)

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□1
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□2
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□3
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□4

Q=8

In case of COM file, maximum length of parameters passed through command line can be…….

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□63 bytes
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□127bytes
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□255 bytes
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□511 bytes

Q=9

We can access the DOS service using;

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Int 0x21
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Int 0x13
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Int 0x 10
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Int 0x 08

Q=10

In 9 pin 9 connector,which pin is assigned to signal ground

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□3
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□4
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□5
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□6

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Q=11:

BPB stands for

- Basic parameter block
- Bios precise block
- Basic precise block
- Bios parameter block

Q=12

Int 13-bios disk service “generally uses which register to return the error flag?

- CF
- DL
- **AH**
- AL

Q=13:

The first sector on the hard disk contains the

- Hard disk size
- Partition table
- Data size
- Sector size

Q=14

Operating system organize data in the form of

- Folder
- Batch file
- File

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- None of above

……

Q=15

In 9 pin db 9 connector, which pin is assigned to TD(transmitted data)

- 1
- 2
- 3
- 4

Q=16”

Device derive can be divided into ----------major categories.

- 5
- 4
- 3
- 2

1. BL contains 5 decimal then after right shift , BL will become

- 3
- 2.5
- 5
- 10

2. 8 * 16 font is stored in _____ bytes.

- 3
- 4
- 8
- ***16***

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3. In DOS input buffer , number of characters actually read on return is stored in

- First byte
- ***Second byte***
- Third byte
- Fourth byte

4. IRQ 0 has priority

- Low
- High
- ***Highest***
- Medium

5. Thread registration code initialize PCB and add to linked list so that _____ will give it turn.

- Assembler
- Linker
- ***Scheduler***
- Debugger

6. Traditional calling conventions are in _____ number

- 1
- **2**
- 3
- 4

7. VESA VEB 2.0 is standard for

- ***High Resolution Mode***
- Low Resolution Mode
- Very High Resolution Mode
- Medium Resolution Mode

8. To clear direction flag which instruction is used

- ***Cld***

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- Clrd
- Cl df
- Clr df

9. In STOSW instruction , When DI is cleared , SI is

- Incremented by 1
- ***Incremented by 2***
- Decremented by 1
- Decremented by 2

10. Interrupt that is used in debugging with help of trap flag is

- INT 0
- ***INT 1***
- INT 2
- INT 3

11. INT for arithmetic overflow is

- INT 1
- INT 2
- INT 3
- ***INT 4***

12. IRQ referred as

- ***Eight Input signals***
- One Input signal
- Eight Output signals
- One output signal

13. IRQ for keyboard is ____***1***_____

14. IRQ for sound card is _____***5***_____

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15. IRQ for floppy disk is _____***6***_____

16. IRQ with highest priority is

- □□□ Keyboard IRQ
- □□□ ***Timer IRQ***
- □□□ Sound Card
- □□□ Floppy Disk

17. Pin for parallel port ground is

- □□□ 10-18
- □□□ ***18-25***
- □□□ 25-32
- □□□ 32-39

18. The physical address of Interrupt Descriptor Table (IDT) is stored in

- □□□ GDTR
- □□□ ***IDTR***
- □□□ IVT
- □□□ IDTT

19. Execution of “RET 2” results in?

20. CX register is

- □□□ ***Count register***
- □□□ Data register
- □□□ Index register
- □□□ Base register

21. OUT instruction uses __**AX**_____ as source register.

22. IN DB-9 connector the Data Set ready pin is at

- □□□ 5
- □□□ ***6***

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- □□□ 7
- □□□ 8

23. If two devices uses same IRQ then there is

- □□□ IRQ collision
- □□□ *IRQ conflict*
- □□□ IRQ drop

24. VESA organizes 16 bit color for every pixel in ratio

- □□□ 5:5:5
- □□□ ***5:6:5***
- □□□ 6:5:6
- □□□ 5:6:7

25. Division by zero is done by which interrupt.

Interrupt 0.

.....

Question No: 1 (M - 1) .

Aft

er the execution of SAR instruction

► **The msb is replaced by a 0**

► The msb is replaced by 1

► The msb retains its original value

► The msb is replaced by the value of CF

Question No: 2 (M - 1) .

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RE

TF will pop the offset in the

- ► BP
- **► IP**
- ► SP
- ► SI

Question No: 3 (M - 1) .

Th

e routine that executes in response to an INT instruction is called

- **► ISR**
- ► IRS
- ► ISP
- ► IRT

Question No: 4 (M - 1) .

Th

e first instruction of “COM” file must be at offset:

- ► 0x0010
- **► 0x0100**
- ► 0x1000
- ► 0x0000

Question No: 5 (M - 1) .

“F

ar” jump is not position relative but is _____

- ► memory dependent
- **► Absolute**
- ► temporary
- ► indirect

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Question No: 6 (M - 1) .

On

ly _____ instructions allow moving data from memory to memory.

► **string**

► word

► indirect

► stack

Question No: 7 (M - 1) .

Aft

er the execution of instruction “RET 2”

► **SP is incremented by 2**

► SP is decremented by 2

► SP is incremented by 4

► SP is decremented by 4

Question No: 8 (M - 1) .

DI

V instruction has

► **Two forms**

► Three forms

► Four forms

► Five forms

Question No: 9 (M - 1) .

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W

hen the operand of DIV instruction is of 16 bits then implied dividend will be of

- ► 8 bits
- ► 16 bits
- ► **32 bits**
- ► 64 bits

Question No: 10 (M - 1) .

Aft

er the execution of MOVS instruction which of the following registers are updated

- ► SI only
- ► DI only
- ► **SI and DI only**
- ► SI, DI and BP only

Question No: 11 (M - 1) .

In

8088 architecture, whenever an element is pushed on the stack

- ► SP is decremented by 1
- ► **SP is decremented by 2**
- ► SP is decremented by 3
- ► SP is decremented by 4

Question No: 12 (M - 1) .

W

hen a very large number is divided by very small number so that the quotient is larger than the space provided, this is called

- ► Divide logical error
- ► **Divide overflow error**

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► Divide syntax error

► An illegal instruction

Question No: 13 (M - 1) .

In the word designated for one screen location, the higher address contains

► The character code

► The attribute byte

► The parameters

► The dimensions

Question No: 14 (M - 1) .

Which of the following options contain the set of instructions to open a window to the video memory?

► mov AX, 0xb008
mov ES, AX

► mov AX, 0xb800
mov ES, AX

► mov AX, 0x8b00
mov ES, AX

► mov AX, 0x800b
mov ES, AX

Question No: 15 (M - 1) .

In a video memory, each screen location corresponds to

► One byte

► Two bytes

► Four bytes

► Eight bytes

Question No: 16 (M - 1) .

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Th

e execution of the instruction “mov word [ES : 0], 0x0741” will print character “A” on screen , background color of the screen will be

► **Black**

► White

► Red

► Blue

Question No: 1 ___(M - 1) .

Which of the following is not true about registers?

1. Their operation is very much like memory
2. Intermediate results may also be stored in registers.
3. They are also called scratch pad ram
4. None of given options.

Question No: 2 ___(M - 1) .

move [bp], al moves the one byte content of the AL register to the address contained in BP register in the current

1. Stack segment
2. Code segment
3. Data segment
4. Extra segment

Question No: 3 (M - 1) .

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In a rotate through carry right (RCR) instruction applied on a 16 bit word

Effectively there is

1. 16 bits rotation
2. 1 bit rotation
3. 17 bits rotation
4. 8 bits rotation

Question No: 4__ (M - 1) - Please

choose one The 8088 stack works on

1. Word sized elements
2. Byte sized elements
3. Double sized element
4. Nible sized element

Question No: 5 (M - 1) - Please

choose one

An 8 x 16 font is stored in……..Bytes

1. 2
2. 4
3. 8
4. 16

Question No: 6 (M - 1) - Please

INT 10 is used for……services.

1. RAM
2. Disk
3. BIOS video

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4. DOS video

Question No: 7 __ (M - 1) .

Priority of IRQ 0 interrupt is

1. medium
2. high
3. highest
4. low

Question No: 8 __ (M - 1) .

Threads can have function calls, parameters and _____ variables.

1. global
2. local
3. legal
4. illegal

Question No: 9 __ (M - 1) - Please choose

one How many prevalent calling conventions do…….exist

1. 1
2. 2
3. 3
4. 4

Question No: 10 (M - 1) - Please choose

one In 9pin DB 9 DSR is assigned on pin number

1. 4
2. 5
3. 6
4. 7

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Question No: 11

(M - 1) - Please

choose one In 9pin DB 9 CTS is assigned on pin

number

1. 6
2. 7
3. 8
4. 9

Question No: 12__ (M - 1) .

In 9pin DB 9 CD is assigned on pin number

1. 1
2. 2
3. 3
4. 4

Question No: 13__ (M - 1) .

In 9pin DB 9 RD is assigned on pin number

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□1
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□2
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□3
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□4

Question No: 14 __ (M - 1) .

in device attribute word which of the following bit decides whether it is a cha rater

1. device or a block device
2. Bit 12 Bit 13

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3. Bit 14
4. Bit 15

Question No: 15__ (M - 1) .

Video servioces are classified into _____broad categories

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□2
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□3
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□4
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□5

Question No: 16 (M - 1) - Please choose

one In STOSB instruction, when DF is clear, SI is

1. Incremented by 1
2. Incremented by 2
3. Decremented by 1
4. Decremented by 2

Question No: 17 (M - 1) . The

process of sending signals back and forth is called

1. Activity
2. Hand-shaking
3. Interruption
4. Time clicking

Question No: 18 (M - 1) .

which of the following is a special type of interrupt that returns to the same instruction instead of the next instruction

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1. Divide overflow interrupt
2. Debug interrupt
3. Arithmetic overflow interrupt
4. Change of sign interrupt

Question No: 19 ___(M - 1) .

Which of the following IRQs is derived by a timer device?

1. IRQ 0
2. IRQ 1
3. IRQ 2
4. IRQ 3

Question No: 20 __ (M - 1) .

Which of the following interrupts is used for Arithmetic overflow

1. INT 1
2. INT 2
3. INT 3
4. INT 4

Question No: 21 __ (M - 1) .

Which of the following IRQs is connected to serial port COM 2?

1. IRQ 0
2. IRQ 1
3. IRQ 2
4. IRQ 3

Question No: 22 __ (M - 1) - Please

choose one

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An End of Interrupt (EOI) signal is sent by

1. Handler
2. Processor
3. IRQ
4. PIC

Question No: 23 __ (M - 1) .

The source registers in OUT is

1. AL or AX
2. BL or BX
3. CL or CX
4. DL or DX

Question No: 24 (M - 1) .

In programmable interrupt controller which of the following ports is used for selectively enabling or disabling interrupts

1. 19
2. 20
3. 21
4. 22

Question No: 25 (M - 1) .

The number of pins in a parallel port connector are?

1. 25
2. 30
3. 35

Question No: 26 (M - 1) .

Which of the following pins of a parallel port connector are grounded?

1. 10-18
2. 18-25
3. 25-32
4. 32-39

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Question No: 27 __ (M - 1) .

Suppose a decimal number 35 when its binary is shifted to write two places the new number will become

1. 35
2. 70
3. 140
4. 17

Question No: 28 __ (M - 1) .

A 32bit address register can access upto .....of memory so memory access has increased a lot.

1. 2GB
2. 4GB
3. 6GB
4. 8GB

Question No: 29 __ (M - 1) .

In NASM an imported symbol is declared with the .....while and exported symbol is declared with the .....

1. Global directive, External directive
2. External directive, Global directive
3. Home Directive, Foreign Directive
4. Foreign Directive, Home Directive

Question No: 30 (M - 1) - Please choose

one Single step interrupt is

1. Hardware interrupt
2. Like divide by zero interrupt

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3. Like divide by 1 interrupt

4. Software interrupt

Question No: 31 __ (M - 1)

Which services are gained bi INT 0x16

Solution:

Hardware interrupt

Like divide by zero interrupt

Like divide by 1 interrupt

Software interrupt

Question No: 32 (M - 1

Give the name of any one VESA servic

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

Question No: 33 (M - 2)
INT 14 - SERIAL - READ CHARACTER FROM PORT
By using above port what do AH,AL and DX shows here?

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

Question No: 34 (M - 2)
What do these instructions do ? write your answer in single line.
mov cx, 0xffff
loop $

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt

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- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

Question No: 35 (M - 3)
Define the protected mode
Solution:

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

Question No: 36 (M - 3)
Write a program in assembly language to disable keyboard interrupt using PIC mask register
Hint: Only five instructions are needed
Solution:

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

Question No: 37 (M - 3)
Read the following passage carefully and fill the blanks with proper words.
Note: Don't rewrite the passage just write the words in same order.
"BIOS sees the disks as a combination of sectors, tracks, and....., as a raw storage device without concern to whether it is reading a file or directory. ..... provides the simplest and most powerful interface to the storage medium. However this raw storage is meaningless to the user who needs to store his files and organize them into..... . "
Solution:

- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Hardware interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by zero interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Like divide by 1 interrupt
- □□□□□□□□□□□□□□□□□□□□□□□□□□□□□Software interrupt

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Question No: 1 (M - 1)

.

Sun SPARC Processor has a fixed _____ instruction size.

1. 16bit
2. 32bit
3. 64bit
4. 20bit

Question No: 2 (M - 1)

.

When the subprogram finishes, the _____ retrieves the return address from the stack and transfers control to that location.

1. RET instruction
2. CALL instruction
3. POP instruction
4. Jump instruction

Question No: 3 (M - 1)

.

A 32 bit address register can access upto _____ of memory.

- 1 GB
- 6 GB
- 4 GB
- 2 GB

Question No: 4 (M - 1)

.

The value of a segment register when the processor is running under protected mode is called

1. segment descriptor
2. segment selector
3. global descriptor table
4. protected register

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Question No: 5 (M - 1)

.

FS and GS are two _____ in protected mode.

1. segment registers
2. segment selectors
3. stack pointers
4. register pointers

Question No: 6 (M - 1)

.

IRQ 0 interrupt have _____ priority

1. low
2. medium
3. highest
4. lowest

Question No: 7 (M - 1)

.

IDT stands for _____.

1. interrupt descriptor table
2. individual descriptor table
3. inline data table
4. interrupt descriptor table

Question No: 8 (M - 1)

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.

Every bit of line status in serial port conveys _____ information.

1. different
2. same
3. partial
4. full

Question No: 9 (M - 1)

.

There are total _____ bytes in a standard floppy disk.

1. 1444k
2. 1440k
3. 1280k
4. 2480k

Question No: 10 (M - 1)

.

An 8x16 font is stored in _____ bytes.

- 8
- 16
- 4
- 20

==========

. Serial Port is also accessible via ***I/O*** ports **, COM 1** is accessible via ports 3F8-3FF while ***COM 2*** is accessible via 2F8 -2FF.

The first register at 3F8 is the ***Transmitter*** holding register if written to and the receiver ***buffer*** register if read from.

Other register of our interest include 3F9 whose ***Bit 0*** must be set to enable received data available interrupt and ***Bit 1*** must be set to enable transmitter holding register empty interrupt.

(Transmitter, COM 1, I/O ports , COM2. bit 0 , Buffer , 3FA)

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Question # 1
There are three busses to communicate the processor and memory named as _____
1) : address bus.,data bus and data bus.
2) : addressing bus.,data bus and data bus.
3) : address bus.,datamove bus and data bus.
4) : address bus.,data bus and control bus..
Correct Option : 4 From : Lecture 1

Question # 2
The address bus is unidirectional and address always travels from processor to memory.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 1

Question # 3
Data bus is bidirectional because_____
1) : To way
2) : Data moves from both, processor to memory and memory to processor,
3) : Data moves from both, processor to memory and memory to data Bus,
4) : None of the Given
Correct Option : 3 From : Lecture 1

Question # 4
Control bus_____
1) : is Not Important.
2) : is Important .
3) : bidirectional.
4) : unidirectional .
Correct Option : 3 From : Lecture 1

Question # 5
A memory cell is an n-bit location to store data, normally _____also called a byte
1) : 4-bit
2) : 8-bit
3) : 6-bit
4) : 80-bit
Correct Option : 2 From : Lecture 1

Question # 6
The number of bits in a cell is called the cell width._____ define the memory completely.
1) : Cell width and number of cells,
2) : cell number and width of the cells,
3) : width
4) : Height
Correct Option : 1 From : Lecture 1

Question # 7
for memory we define two dimensions. The first dimension defines how many _____bits are there in a single memory cell.
1) : parallel
2) : Vertical

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3) : long
4) : short
Correct Option : 1 From : Lecture 1

Question # 8
_____ operation requires the same size of data bus and memory cell width.
1) : Normal
2) : Best and simplest
3) : first
4) : None of the Given
Correct Option : 2 From : Lecture 1

Question # 9
Control bus is only the mechanism. The responsibility of sending the appropriate signals on the control bus to the memory is of the_____.
1) : Data Bus
2) : processor
3) : Address Bus
4) : None of the Given
Correct Option : 2 From : Lecture 1

Question # 10
In “total: dw 0 ” Opcode total is a _____
1) : Literal
2) : Variable
3) : Label
4) : Starting point
Correct Option : 3 From : Lecture 10

Question # 11
| 0 |-->| 1 | 1 | 0 | 1 | 0 | 0 | 0 | -->| C | is a example of _____
1) : Shl
2) : sar
3) : Shr
4) : Sal
Correct Option : 3 From : Lecture 10

Question # 12
| C |<--| 1 | 1 | 0 | 1 | 0 | 0 | 0 | <--| 0 | is a example of _____
1) : Shl
2) : sar
3) : Shr
4) : Sal
Correct Option : 1 From : Lecture 10

Question # 13
ADC has _____ operands.
1) : two
2) : three
3) : Five
4) : Zero
Correct Option : 2 From : Lecture 10

Question # 14
The basic purpose of a computer is to perform operations, and operations need _____.
1) : order

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2) : nothing
3) : operands
4) : bit
Correct Option : 3 From : Lecture 2

Question # 15
Registers are like a scratch pad ram inside the processor and their operation is very much like normal_____.
1) : Number
2) : opreations
3) : memory cells
4) : None of the Given
Correct Option : 3 From : Lecture 2

Question # 16
There is a central register in every processor called the _____ and The word size of a processor is defined by the width of its_____.
1) : accumulator,accumulator
2) : data bus,accumulator
3) : accumulator, Address Bus
4) : accumulator,memory
Correct Option : 1 From : Lecture 2

Question # 17
_____does not hold data but holds the address of data
1) : Pointer, Segment, or Base Register
2) : Pointer, Index, or Base Register
3) : General Registers
4) : Instruction Pointer
Correct Option : 2 From : Lecture 2

Question # 18
“The program counter holds the address of the next instruction to be _____”
1) : executed.
2) : called
3) : deleted
4) : copy
Correct Option : 1 From : Lecture 2

Question # 19
There are _____ types of “instruction groups”
1) : 4
2) : 5
3) : 3
4) : 2
Correct Option : 1 From : Lecture 2

Question # 20
These instructions are used to move data from one place to another.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 2

Question # 21

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“mov” instruction is related to the _____ *****.
1) : Arithmetic and Logic Instructions
2) : Data Movement Instructions
3) : Program Control Instructions
4) : Special Instructions
Correct Option : 2 From : Lecture 2

Question # 22
_____allow changing specific processor behaviors and are used to play with it.
1) : Special Instructions
2) : Data Movement Instructions
3) : Program Control Instructions
4) : Arithmetic and Logic Instructions
Correct Option : 1 From : Lecture 2

Question # 23
8088 is a 16bit processor with its accumulator and all registers of _____.
1) : 32 bits
2) : 6 bits
3) : 16 bits
4) : 64 bits
Correct Option : 3 From : Lecture 2

Question # 24
The _____ of a processor means the organization and functionalities of the registers it contains and the instructions that are valid on the processor.
1) : Manufactures
2) : architecture
3) : Deal
4) : None of the Given
Correct Option : 2 From : Lecture 2

Question # 25
Intel IAPX88 Architecture is _____
1) : More then 25 old
2) : New
3) : Not Good
4) : None of the Given
Correct Option : 1 From : Lecture 2

Question # 26
The iAPX88 architecture consists of_____registers.
1) : 13
2) : 12
3) : 9
4) : 14
Correct Option : 4 From : Lecture 3

Question # 27
General Registers are _____
1) : AX, BX, CX, and DX
2) : XA, BX, CX, and DX
3) : SS,SI and DI
4) : 3
Correct Option : 1 From : Lecture 3

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Question # 28
AX means we are referring to the extended 16bit “A” register. Its upper and lower byte are separately accessible as _____.
1) : AH and AL
2) : A Lower and A Upper
3) : AL, AU
4) : AX
Correct Option : 1 From : Lecture 3

Question # 29
AX is General purpose Register where A stands for_____.
1) : Acadmic
2) : Ado
3) : Architecture
4) : Accumulator
Correct Option : 4 From : Lecture 3

Question # 30
The B of BX stands for _____because of its role in memory addressing.
1) : Busy
2) : Base
3) : Better
4) : None of the Given
Correct Option : 2 From : Lecture 3

Question # 31
The D of DX stands for Destination as it acts as the destination in _____.
1) : I/O operations
2) : operations
3) : memory cells
4) : Memory I/O operations
Correct Option : 1 From : Lecture 3

Question # 32
The C of CX stands for Counter as there are certain instructions that work with an automatic count in the _____.
1) : DI register
2) : BX register
3) : CX register
4) : DX register
Correct Option : 3 From : Lecture 3

Question # 33
_____are the index registers of the Intel architecture which hold address of data and used in memory access.
1) : SI and SS
2) : PI and DI
3) : SI and IP
4) : SI and DI
Correct Option : 4 From : Lecture 3

Question # 34
In Intel IAPX88 architecture _____ is the special register containing the address of the next instruction to be executed.
1) : AX
2) : PI

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3) : IP
4) : SI
Correct Option : 3 From : Lecture 3

Question # 35
SP is a memory pointer and is used indirectly by a set of _____.
1) : instructions
2) : Pointers
3) : Indexes
4) : Variables
Correct Option : 1 From : Lecture 3

Question # 36
_____is also a memory pointer containing the address in a special area of memory called the stack.
1) : SP
2) : BP
3) : PB
4) : AC
Correct Option : 2 From : Lecture 3

Question # 37
_____is bit wise significant and accordingly each bit is named separately.
1) : AX
2) : FS
3) : IP
4) : Flags Register
Correct Option : 4 From : Lecture 3

Question # 38
When two 16bit numbers are added the answer can be 17 bits long, this extra bit that won't fit in the target register is placed in the _____where it can be used and tested
1) : carry flag
2) : Parity Flag
3) : Auxiliary Carry
4) : Zero Flag
Correct Option : 1 From : Lecture 3

Question # 39
Program is an ordered set of instructions for the processor.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3

Question # 40
For Intel Architecture "operation destination, source" is way of writing things.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3

Question # 41
Operation code " add ax, bx " _____.

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1) : Add the bx to ax and change the bx
2) : Add the ax to bx and change the ax
3) : Add the bx to ax and change the ax
4) : Add the bx to ax and change nothing
Correct Option : 3 From : Lecture 3

Question # 42
The maximum memory iAPX88 can access is_____.
1) : 1MB
2) : 2MB
3) : 3MB
4) : 128MB
Correct Option : 1 From : Lecture 4

Question # 43
The maximum memory iAPX88 can access is 1MB which can be accessed with _____.
1) : 18 bits
2) : 20 bits
3) : 16 bits
4) : 2 bits
Correct Option : 2 From : Lecture 4

Question # 44
_____address of 1DED0 where the opcode B80500 is placed.
1) : physical memory
2) : memory
3) : efective
4) : None of the Given
Correct Option : 1 From : Lecture 4

Question # 45
16 bit of Segment and Offset Addresses can be converted to 20bit Address i.e
Segment Address with lower four bits zero + Offset Address with _____ four bits zero = 20bit Physical Address
1) : Middle
2) : lower
3) : Top
4) : upper
Correct Option : 4 From : Lecture 4

Question # 46
When adding two 20bit Addresses a carry if generated is dropped without being stored anywhere and the phenomenon is called address_____.
1) : wraparound
2) : mode
3) : ping
4) : error
Correct Option : 1 From : Lecture 4

Question # 47
segments can only be defined a 16byte boundaries called _____ boundaries.
1) : segment
2) : paragraph
3) : Cell
4) : RAM
Correct Option : 1 From : Lecture 4

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Question # 48
in a Program CS, DS, SS, and ES all had the same value in them. This is called _____.
1) : equel memory
2) : overlapping segments
3) : segments hidding
4) : overlapping SI
Correct Option : 2 From : Lecture 4

Question # 49
“db num1” size of the memory is _____
1) : 1byte
2) : 4bit
3) : 16bit
4) : 2byte
Correct Option : 1 From : Lecture 5

Question # 50
“ 1----------[org 0x0100]
2----------mov ax, [num1] ; load first number in ax
3----------mov bx, [num2] ; load second number in bx
4----------add ax, bx _____
5----------int 0x21
6----------
7----------num1: dw 5
8----------num2: dw 10

Comments for the 4 are :
1) : No comments Will be
2) : ; accumulate sum in add
3) : ; accumulate sum in ax
4) : ; accumulate sum in Bx
Correct Option : 3 From : Lecture 5

Question # 51
In “ mov ax, bx ” is _____ Addressing Modes.
1) : Immediate
2) : Indirect
3) : Direct
4) : Register
Correct Option : 4 From : Lecture 5

Question # 52
In “mov ax, [bx] ” is _____ Addressing Modes
1) : Based Register Indirect
2) : Indirect
3) : Base Indirect
4) : Immediate
Correct Option : 1 From : Lecture 5

Question # 53
In “mov ax, 5 ” is _____ Addressing Modes
1) : Immediate
2) : Indirect

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3) : Indirect
4) : Register
Correct Option : 1 From : Lecture 6

Question # 54
In " mov ax, [num1+bx] " is _____ ADDRESSING
1) : OFFSET+ Indirect
2) : Register + Direct
3) : Indirect + Reference
4) : BASEd REGISTER + OFFSET
Correct Option : 4 From : Lecture 7

Question # 55
"base + offset addressing " gives This number which came as the result of addition is called the _____.
1) : Address
2) : mode
3) : effective address
4) : Physical Address
Correct Option : 3 From : Lecture 7

Question # 56
"mov ax, [cs:bx]" associates _____ for this one instruction
1) : CS with BX
2) : BX with CS
3) : BX with AX
4) : None of the Given
Correct Option : 2 From : Lecture 7

Question # 57
For example
BX=0100
DS=FFF0
And Opcode are;
move [bx+0x0100], Ax
now what is the effective memory address;
1) : 0020
2) : 0200
3) : 0300
4) : 0x02
Correct Option : 2 From : Lecture 7

Question # 58
For example
BX=0100
DS=FFF0
And Opcode are;
move [bx+0x0100], Ax
now what is the physical memory address;
1) : 0020
2) : 0x0100
3) : 0x10100
4) : 0x100100
Correct Option : 2 From : Lecture 7

Question # 59

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In “ mov [1234], al ” is _____ Addressing Modes.
1) : Immediate
2) : Indirect
3) : Direct
4) : Register
Correct Option : 3 From : Lecture 8

Question # 60
In “ mov [SI], AX ” is _____ Addressing Modes.
1) : Basef Register Indirect
2) : Indirect
3) : Indexed Register Indirect
4) : Immediate
Correct Option : 3 From : Lecture 8

Question # 61
In “ mov ax, [bx - Si] ” is _____ ADDRESSING
1) : Basef Register Indirect
2) : Indirect
3) : Direct
4) : illegal
Correct Option : 4 From : Lecture 8

Question # 62
In “ mov ax, [BL] ” there is error i.e. _____
1) : Address must be 16bit
2) : Address must be 8bit
3) : Address must be 4bit
4) : 8 bit to 16 bit move illegal
Correct Option : 4 From : Lecture 8

Question # 63
In “ mov ax, [SI+DI] ” there is error i.e. _____
1) : Two indexes can’t use as Memory Address
2) : index can’t use as Memory Address
3) : I don't Know
4) : None of the Given
Correct Option : 1 From : Lecture 8

Question # 64
In JNE and JNZ there is difference for only _____;
1) : Programmer or Logic
2) : Assembler
3) : Debugger
4) : IAPX88
Correct Option : 1 From : Lecture 9

Question # 65
JMP is Instruction that on executing take jump regardless of the state of all flags is called_____
1) : Jump
2) : Conditional jump
3) : Unconditional jump
4) : Stay
Correct Option : 3 From : Lecture 9

Question # 66

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When result of the source subtraction from the destination is zero, zero flag is set i.e. ZF=1
its mean that;
1) : DEST = SRC
2) : DEST != SRC
3) : DEST < SRC
4) : DEST > SRC
Correct Option : 1 From : Lecture 9

Question # 67
When an unsigned source is subtracted from an unsigned destination and the destination is smaller, borrow is needed which sets the _____.
1) : carry flag i.e CF = 0
2) : carry flag i.e CF = 1
3) : Carry Flag + ZF=1
4) : None of the Given
Correct Option : 2 From : Lecture 9

Question # 68
In the case of unassigned source and destination when subtracting and in the result ZF =1 OR CR=1 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST ? USRC
4) : DEST > SRC
Correct Option : 3 From : Lecture 9

Question # 69
In the case of unassigned source and destination when subtracting and in the result ZF =0 AND CR=0 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST < USRC
4) : UDEST > USRC
Correct Option : 4 From : Lecture 9

Question # 70
In the case of unassigned source and destination when subtracting and in the result CR=0 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST < USRC
4) : UDEST ? USRC
Correct Option : 4 From : Lecture 9

Question # 71
_____This jump is taken if the last arithmetic operation produced a zero in its destination. After a CMP it is taken if both operands were equal.
1) : Jump if zero(JZ)/Jump if equal(JE)
2) : Jump if equal(JE)
3) : Jump if zero(JZ)
4) : No Jump fot This
Correct Option : 1 From : Lecture 9

Question # 72
_____This jump is taken after a CMP if the unsigned source is smaller than or equal to the unsigned destination.

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1) : JBE(Jump if not below or equal)
2) : JNA(Jump if not above)/JBE(Jump if not below or equal)
3) : JNA(Jump if not above)
4) : No Jump fot This
Correct Option : 2 From : Lecture 9
Question # 1
Numbers of any size can be added using a proper combination of _____.
1) : ADD and ADC
2) : ABD and ADC
3) : ADC and ADC
4) : None of the Given
Correct Option : 1 From : Lecture 11

Question # 2
Like addition with carry there is an instruction to subtract with borrows called_____.
1) : SwB
2) : SBB
3) : SBC
4) : SBBC
Correct Option : 2 From : Lecture 11

Question # 3
if “and ax, bx” instruction is given, There are _____ operations as a result
1) : 16 AND
2) : 17 AND
3) : 32 AND
4) : 8 AND
Correct Option : 1 From : Lecture 12

Question # 4
_____can be used to check whether particular bits of a number are set or not.
1) : AND
2) : OR
3) : XOR
4) : NOT
Correct Option : 1 From : Lecture 12

Question # 5
_____can also be used as a masking operation to invert selective bits.
1) : AND
2) : OR
3) : XOR
4) : NOT
Correct Option : 3 From : Lecture 12

Question # 6
Masking Operations are Selective Bit _____
1) : Clearing, XOR, Inversion and Testing
2) : Clearing, Setting, Inversion and Testing
3) : Clearing, XOR, AND and Testing
4) : None of the Given
Correct Option : 2 From : Lecture 12

Question # 7
The _____ instruction allows temporary diversion and therefore reusability of code.
1) : CALL

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2) : RET
3) : AND
4) : XOR
Correct Option : 1 From : Lecture 13

Question # 8
CALL takes a label as _____ and execution starts from that label,
1) : argument
2) : Lable
3) : TXt
4) : Register
Correct Option : 1 From : Lecture 13

Question # 9
When the _____instruction is encountered and it takes execution back to the instruction following the CALL.
1) : CALL
2) : RET
3) : AND
4) : XOR
Correct Option : 2 From : Lecture 13

Question # 10
_____ Both the instructions are commonly used as a pair, however technically they are independent in their operation.
1) : RET and ADC
2) : Cal and SSb
3) : CALL and RET
4) : ADC and SSB
Correct Option : 3 From : Lecture 13

Question # 11
The CALL mechanism breaks the thread of execution and does not change registers, except _____.
1) : SI
2) : IP
3) : DI
4) : SP
Correct Option : 2 From : Lecture 13

Question # 12
Stack is a _____ that behaves in a first in last out manner.
1) : Program
2) : data structure
3) : Heap
4) : None of the Given
Correct Option : 2 From : Lecture 14

Question # 13
If _____ is not available, stack clearing by the callee is a complicated process.
1) : CALL
2) : SBB
3) : RET n
4) : None of the Given
Correct Option : 3 From : Lecture 14

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Question # 14
When the stack will eventually become full, SP will reach 0, and thereafter wraparound producing unexpected results. This is called stack _____
1) : Overflow
2) : Leakage
3) : Error
4) : Pointer
Correct Option : 1 From : Lecture 14

Question # 15
The pop operation makes a copy from the top of the stack into its_____.
1) : Register
2) : operand
3) : RET n
4) : Pointer
Correct Option : 2 From : Lecture 14

Question # 16
_____decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack
1) : PUSH
2) : POP
3) : CALL
4) : RET
Correct Option : 1 From : Lecture 14

Question # 17
POP transfers the word at the current top of stack (pointed to by SP) to the destination operand and then _____ SP by two to point to the new top of stack.
1) : increments
2) : dcrements
3) : ++
4) : --
Correct Option : 1 From : Lecture 14

Question # 18
The trick is to use the _____and _____operations and save the callers' value on the stack and recover it from there on return.
1) : POP, ADC
2) : CALL, RET
3) : CALL, RET n
4) : PUSH, POP
Correct Option : 4 From : Lecture 14

Question # 19
To access the arguments from the stack, the immediate idea that strikes is to _____ them off the stack.
1) : PUSH
2) : POP
3) : CALL
4) : Rrgister
Correct Option : 2 From : Lecture 15

Question # 20
push bp
we are _____

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1) : sending bp copy to stack
2) : making bp copy from stack
3) : pushing bp on the stack
4) : doing nothing
Correct Option : 3 From : Lecture 15

Question # 21
Local Variables means variables that are used within the _____
1) : Subroutine
2) : Program
3) : CALL
4) : Label
Correct Option : 1 From : Lecture 15

Question # 22
Standard ASCII has 128 characters with assigned numbers from _____.
1) : 1to 129
2) : 0 to 127
3) : 0 to 128
4) : None of the Given
Correct Option : 2 From : Lecture 16

Question # 23
When _____ is sent to the VGA card, it will turn pixels on and off in such a way that a visual representation of ‘A’ appears on the screen.
1) : 0x60
2) : 0x90
3) : 0x30
4) : 0x40
Correct Option : 4 From : Lecture 16

Question # 24
Which bit is refer to the Blinking of foreground character
1) : 6
2) : 7
3) : 5
4) : 3
Correct Option : 2 From : Lecture 16

Question # 25
Which bit is refer to the Intensity component of foreground color
1) : 4
2) : 5
3) : 3
4) : 7
Correct Option : 3 From : Lecture 16

Question # 26
Which bit is refer to the Green component of background color
1) : 1
2) : 5
3) : 3
4) : 7
Correct Option : 2 From : Lecture 16

Question # 27

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Which bit is refer to the Green component of foreground color
1) : 1
2) : 5
3) : 3
4) : 7
Correct Option : 1 From : Lecture 16

Question # 28
String can be indicate bye given
1) : db 0x61, 0x61, 0x63
2) : db 'a', 'b', 'c'
3) : db 'abc'
4) : All of the above
Correct Option : 4 From : Lecture 16

Question # 29
The first form divides a 32bit number in DX:AX by its 16bit operand and stores the _____ quotient in AX
1) : 16bit
2) : 17bit
3) : 32bit
4) : 64bit
Correct Option : 1 From : Lecture 17

Question # 30
The _____ (division) used in the process is integer division and not floating point division.
1) : DIV instruction
2) : ADC instruction
3) : SSB instruction
4) : DIVI instruction
Correct Option : 1 From : Lecture 17

Question # 31
_____(multiply) performs an unsigned multiplication of the source operand and the accumulator.
1) : Multi
2) : DIV
3) : MUL
4) : Move
Correct Option : 3 From : Lecture 18

Question # 32
The desired location on the screen can be calculated with the following formulae.
1) : location = (hypos * 80 + SP) * 3
2) : location = (hypos * 80 + slocation) * 2
3) : location = (hypos * 80 + epos) * 2
4) : None of the Given
Correct Option : 3 From : Lecture 18

Question # 33
To play with string there are 5 instructions that are _____
1) : STOS, LODS, CMPS, SCAS, and MOVS
2) : MUL, DIV, ADD, ADC and MOVE
3) : SSB, ADD, CMPS, ADC, and MOVS
4) : None of the Given
Correct Option : 1 From : Lecture 18

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Question # 34
_____transfers a byte or word from register AL or AX to the string element addressed by ES:DI and updates DI to point to the next location.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 2 From : Lecture 18

Question # 35
_____ transfers a byte or word from the source location DS:SI to AL or AX and updates SI to point to the next location.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 1 From : Lecture 18

Question # 36
_____compares a source byte or word in register AL or AX with the destination string element addressed by ES: DI and updates the flags.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 3 From : Lecture 18

Question # 37
_____ repeat the following string instruction while the zero flag is set and REPNE or REPNZ repeat the following instruction while the zero flag is not set.
1) : REP or REPZ
2) : REPE or REPZ
3) : REPE or RPZ
4) : RPE or REPZ
Correct Option : 2 From : Lecture 18

Question # 38
LES loads _____
1) : ES
2) : DS
3) : PS
4) : LS
Correct Option : 1 From : Lecture 20

Question # 39
LDS loads_____.
1) : ES
2) : DS
3) : PS
4) : LS
Correct Option : 2 From : Lecture 20

Question # 40
REP allows the instruction to be repeated _____ times allowing blocks of memory to be copied.

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1) : DX
2) : CX
3) : BX
4) : AX
Correct Option : 2 From : Lecture 20

Question # 41
_____pops IP, then CS, and then FLAGS.
1) : Ret n
2) : REZA
3) : REPE
4) : IRET
Correct Option : 4 From : Lecture 21

Question # 42
_____ , Trap, Single step Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 2 From : Lecture 21

Question # 43
_____,NMI-Non Maskable Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 3 From : Lecture 21

Question # 44
To hook an interrupt we change the _____ corresponding to that interrupt.
1) : SX
2) : vector
3) : AX
4) : BX
Correct Option : 2 From : Lecture 22
Question # 1
_____pops IP, then CS, and then FLAGS.
1) : Ret n
2) : REZA
3) : REPE
4) : IRET
Correct Option : 4 From : Lecture 21

Question # 2
_____ , Trap, Single step Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 2 From : Lecture 21

Question # 3
_____,NMI-Non Maskable Interrupt
1) : INT 0

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2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 3 From : Lecture 21

Question # 4
To hook an interrupt we change the _____ corresponding to that interrupt.
1) : SX
2) : vector
3) : AX
4) : BX

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Question # 1
There are three busses to communicate the processor and memory named as _____
1) : address bus.,data bus and data bus.
2) : addressing bus.,data bus and data bus.
3) : address bus.,datamove bus and data bus.
4) : address bus.,data bus and control bus..
Correct Option : 4 From : Lecture 1

Question # 2
The address bus is unidirectional and address always travels from processor to memory.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 1

Question # 3
Data bus is bidirectional because_____
1) : To way
2) : Data moves from both, processor to memory and memory to processor,

3) : Data moves from both, processor to memory and memory to data Bus,
4) : None of the Given
Correct Option : 3 From : Lecture 1

Question # 4
Control bus_____
1) : is Not Important.
2) : is Important .
3) : bidirectional.
4) : unidirectional .
Correct Option : 3 From : Lecture 1

Question # 5
A memory cell is an n-bit location to store data, normally _____also called a byte
1) : 4-bit
2) : 8-bit
3) : 6-bit
4) : 80-bit
Correct Option : 2 From : Lecture 1

Question # 6
The number of bits in a cell is called the cell width._____ define the memory completely.
1) : Cell width and number of cells,
2) : cell number and width of the cells,
3) : width
4) : Height
Correct Option : 1 From : Lecture 1

Question # 7
for memory we define two dimensions. The first dimension defines how many _____bits are there in a single memory cell.
1) : parallel
2) : Vertical
3) : long
4) : short
Correct Option : 1 From : Lecture 1

Question # 8
_____ operation requires the same size of data bus and memory cell width.
1) : Normal
2) : Best and simplest
3) : first
4) : None of the Given
Correct Option : 2 From : Lecture 1

Question # 9
Control bus is only the mechanism. The responsibility of sending the appropriate signals on the control bus to the memory is of the_____.
1) : Data Bus
2) : processor
3) : Address Bus
4) : None of the Given
Correct Option : 2 From : Lecture 1

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Question # 10
In “total: dw 0 ” Opcode total is a _____
1) : Literal
2) : Variable
3) : Label
4) : Starting point
Correct Option : 3 From : Lecture 10

Question # 11
| 0 |-->| 1 | 1 | 0 | 1 | 0 | 0 | 0 | -->| C | is a example of _____
1) : Shl
2) : sar
3) : Shr
4) : Sal
Correct Option : 3 From : Lecture 10

Question # 12
| C |‹--| 1 | 1 | 0 | 1 | 0 | 0 | 0 | ‹--| 0 | is a example of _____
1) : Shl
2) : sar
3) : Shr
4) : Sal
Correct Option : 1 From : Lecture 10

Question # 13
ADC has _____ operands.
1) : two
2) : three
3) : Five
4) : Zero
Correct Option : 2 From : Lecture 10

Question # 14
The basic purpose of a computer is to perform operations, and operations need _____.
1) : order
2) : nothing
3) : operands
4) : bit
Correct Option : 3 From : Lecture 2

Question # 15
Registers are like a scratch pad ram inside the processor and their operation is very much like normal_____.
1) : Number
2) : opreations
3) : memory cells
4) : None of the Given
Correct Option : 3 From : Lecture 2
Question # 16
There is a central register in every processor called the _____ and The word size of a processor is defined by the width of its_____.
1) : accumulator,accumulator
2) : data bus,accumulator
3) : accumulator, Address Bus
4) : accumulator,memory

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Correct Option : 1 From : Lecture 2

Question # 17
_____does not hold data but holds the address of data
1) : Pointer, Segment, or Base Register
2) : Pointer, Index, or Base Register
3) : General Registers
4) : Instruction Pointer
Correct Option : 2 From : Lecture 2

Question # 18
“The program counter holds the address of the next instruction to be _____”
1) : executed.
2) : called
3) : deleted
4) : copy
Correct Option : 1 From : Lecture 2
Question # 19
There are _____ types of “instruction groups”
1) : 4
2) : 5
3) : 3
4) : 2
Correct Option : 1 From : Lecture 2
Question # 20
These instructions are used to move data from one place to another.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 2

Question # 21
“mov” instruction is related to the _____ Group.
1) : Arithmetic and Logic Instructions
2) : Data Movement Instructions
3) : Program Control Instructions
4) : Special Instructions
Correct Option : 2 From : Lecture 2

Question # 22
_____allow changing specific processor behaviors and are used to play with it.
1) : Special Instructions
2) : Data Movement Instructions
3) : Program Control Instructions
4) : Arithmetic and Logic Instructions
Correct Option : 1 From : Lecture 2
Question # 23
8088 is a 16bit processor with its accumulator and all registers of _____.
1) : 32 bits
2) : 6 bits
3) : 16 bits
4) : 64 bits
Correct Option : 3 From : Lecture 2

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Question # 24
The _____ of a processor means the organization and functionalities of the registers it contains and the instructions that are valid on the processor.
1) : Manufactures
2) : architecture
3) : Deal
4) : None of the Given
Correct Option : 2 From : Lecture 2
Question # 25
Intel IAPX88 Architecture is _____
1) : More then 25 old
2) : New
3) : Not Good
4) : None of the Given
Correct Option : 1 From : Lecture 2

Question # 26
The iAPX88 architecture consists of_____registers.
1) : 13
2) : 12
3) : 9
4) : 14
Correct Option : 4 From : Lecture 3
Question # 27
General Registers are _____
1) : AX, BX, CX, and DX
2) : XA, BX, CX, and DX
3) : SS,SI and DI
4) : 3
Correct Option : 1 From : Lecture 3

Question # 28
AX means we are referring to the extended 16bit “A” register. Its upper and lower byte are separately accessible as _____.
1) : AH and AL
2) : A Lower and A Upper
3) : AL, AU
4) : AX
Correct Option : 1 From : Lecture 3

Question # 29
AX is General purpose Register where A stands for_____.
1) : Acadmic
2) : Ado
3) : Architecture
4) : Accumulator
Correct Option : 4 From : Lecture 3

Question # 30
The B of BX stands for _____because of its role in memory addressing.
1) : Busy
2) : Base
3) : Better
4) : None of the Given

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Correct Option : 2 From : Lecture 3

Question # 31
The D of DX stands for Destination as it acts as the destination in _____.
1) : I/O operations
2) : operations
3) : memory cells
4) : Memory I/O operations
Correct Option : 1 From : Lecture 3

Question # 32
The C of CX stands for Counter as there are certain instructions that work with an automatic count in the _____.
1) : DI register
2) : BX register
3) : CX register
4) : DX register
Correct Option : 3 From : Lecture 3

Question # 33
_____are the index registers of the Intel architecture which hold address of data and used in memory access.
1) : SI and SS
2) : PI and DI
3) : SI and IP
4) : SI and DI
Correct Option : 4 From : Lecture 3

Question # 34
In Intel IAPX88 architecture _____ is the special register containing the address of the next instruction to be executed.
1) : AX
2) : PI
3) : IP
4) : SI
Correct Option : 3 From : Lecture 3

Question # 35
SP is a memory pointer and is used indirectly by a set of _____.
1) : instructions
2) : Pointers
3) : Indexes
4) : Variables
Correct Option : 1 From : Lecture 3

Question # 36
_____is also a memory pointer containing the address in a special area of memory called the stack.
1) : SP
2) : BP
3) : PB
4) : AC
Correct Option : 2 From : Lecture 3
Question # 37
_____is bit wise significant and accordingly each bit is named

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separately.
1) : AX
2) : FS
3) : IP
4) : Flags Register
Correct Option : 4 From : Lecture 3

Question # 38
When two 16bit numbers are added the answer can be 17 bits long, this extra bit that won't fit in the target register is placed in the _____where it can be used and tested
1) : carry flag
2) : Parity Flag
3) : Auxiliary Carry
4) : Zero Flag
Correct Option : 1 From : Lecture 3
Question # 39
Program is an ordered set of instructions for the processor.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3
Question # 40
For Intel Architecture "operation destination, source" is way of writing things.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3

Question # 41
Operation code " add ax, bx " _____.
1) : Add the bx to ax and change the bx
2) : Add the ax to bx and change the ax
3) : Add the bx to ax and change the ax
4) : Add the bx to ax and change nothing
Correct Option : 3 From : Lecture 3

Question # 42
The maximum memory iAPX88 can access is_____.
1) : 1MB
2) : 2MB
3) : 3MB
4) : 128MB
Correct Option : 1 From : Lecture 4
Question # 43
The maximum memory iAPX88 can access is 1MB which can be accessed with _____.
1) : 18 bits
2) : 20 bits
3) : 16 bits
4) : 2 bits
Correct Option : 2 From : Lecture 4

Question # 44

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_____address of 1DED0 where the opcode B80500 is placed.
1) : physical memory
2) : memory
3) : efective
4) : None of the Given
Correct Option : 1 From : Lecture 4

Question # 45
16 bit of Segment and Offset Addresses can be converted to 20bit Address i.e Segment Address with lower four bits zero + Offset Address with _____ four bits zero = 20bit Physical Address
1) : Middle
2) : lower
3) : Top
4) : upper
Correct Option : 4 From : Lecture 4

Question # 46
When adding two 20bit Addresses a carry if generated is dropped without being stored anywhere and the phenomenon is called address_____.
1) : wraparound
2) : mode
3) : ping
4) : error
Correct Option : 1 From : Lecture 4

Question # 47
segments can only be defined a 16byte boundaries called _____ boundaries.
1) : segment
2) : paragraph
3) : Cell
4) : RAM
Correct Option : 1 From : Lecture 4

Question # 48
in a Program CS, DS, SS, and ES all had the same value in them. This is called _____.
1) : equel memory
2) : overlapping segments
3) : segments hidding
4) : overlapping SI
Correct Option : 2 From : Lecture 4

Question # 49
“db num1” size of the memory is _____
1) : 1byte
2) : 4bit
3) : 16bit
4) : 2byte
Correct Option : 1 From : Lecture 5
Question # 50
“ 1----------[org 0x0100]
2----------mov ax, [num1] ; load first number in ax
3----------mov bx, [num2] ; load second number in bx

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4----------add ax, bx _____
5----------int 0x21
6----------
7----------num1: dw 5
8----------num2: dw 10

Comments for the 4 are :
1) : No comments Will be
2) : ; accumulate sum in add
3) : ; accumulate sum in ax
4) : ; accumulate sum in Bx
Correct Option : 3 From : Lecture 5

Question # 51
In " mov ax, bx " is _____ Addressing Modes.
1) : Immediate
2) : Indirect
3) : Direct
4) : Register
Correct Option : 4 From : Lecture 5

Question # 52
In "mov ax, [bx] " is _____ Addressing Modes
1) : Based Register Indirect
2) : Indirect
3) : Base Indirect
4) : Immediate
Correct Option : 1 From : Lecture 5

Question # 53
In "mov ax, 5 " is _____ Addressing Modes
1) : Immediate
2) : Indirect
3) : Indirect
4) : Register
Correct Option : 1 From : Lecture 6

Question # 54
In " mov ax, [num1+bx] " is _____ ADDRESSING
1) : OFFSET+ Indirect
2) : Register + Direct
3) : Indirect + Reference
4) : BASEd REGISTER + OFFSET
Correct Option : 4 From : Lecture 7

Question # 55
"base + offset addressing " gives This number which came as the result of addition is called the _____.
1) : Address
2) : mode
3) : effective address
4) : Physical Address
Correct Option : 3 From : Lecture 7

Question # 56

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“mov ax, [cs:bx]” associates _____ for this one instruction
1) : CS with BX
2) : BX with CS
3) : BX with AX
4) : None of the Given
Correct Option : 2 From : Lecture 7

Question # 57
For example
BX=0100
DS=FFF0
And Opcode are;
move [bx+0x0100], Ax
now what is the effective memory address;
1) : 0020
2) : 0200
3) : 0300
4) : 0x02
Correct Option : 2 From : Lecture 7
Question # 58
For example
BX=0100
DS=FFF0
And Opcode are;
move [bx+0x0100], Ax
now what is the physical memory address;
1) : 0020
2) : 0x0100
3) : 0x10100
4) : 0x100100
Correct Option : 2 From : Lecture 7

Question # 59
In “ mov [1234], al ” is _____ Addressing Modes.
1) : Immediate
2) : Indirect
3) : Direct
4) : Register
Correct Option : 3 From : Lecture 8

Question # 60
In “ mov [SI], AX ” is _____ Addressing Modes.
1) : Basef Register Indirect
2) : Indirect
3) : Indexed Register Indirect
4) : Immediate
Correct Option : 3 From : Lecture 8

Question # 61
In “ mov ax, [bx - Si] ” is _____ ADDRESSING
1) : Basef Register Indirect
2) : Indirect
3) : Direct
4) : illegal
Correct Option : 4 From : Lecture 8

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Question # 62
In “ mov ax, [BL] ” there is error i.e. _____
1) : Address must be 16bit
2) : Address must be 8bit
3) : Address must be 4bit
4) : 8 bit to 16 bit move illegal
Correct Option : 4 From : Lecture 8

Question # 63
In “ mov ax, [SI+DI] ” there is error i.e. _____
1) : Two indexes can’t use as Memory Address
2) : index can’t use as Memory Address
3) : I don't Know
4) : None of the Given
Correct Option : 1 From : Lecture 8

Question # 64
In JNE and JNZ there is difference for only _____;
1) : Programmer or Logic
2) : Assembler
3) : Debugger
4) : IAPX88
Correct Option : 1 From : Lecture 9

Question # 65
JMP is Instruction that on executing take jump regardless of the state of all flags is called_____
1) : Jump
2) : Conditional jump
3) : Unconditional jump
4) : Stay
Correct Option : 3 From : Lecture 9
Question # 66
When result of the source subtraction from the destination is zero, zero flag is set i.e. ZF=1
its mean that;
1) : DEST = SRC
2) : DEST != SRC
3) : DEST < SRC
4) : DEST > SRC
Correct Option : 1 From : Lecture 9
Question # 67
When an unsigned source is subtracted from an unsigned destination and the destination is smaller, borrow is needed which sets the _____.
1) : carry flag i.e CF = 0
2) : carry flag i.e CF = 1
3) : Carry Flag + ZF=1
4) : None of the Given
Correct Option : 2 From : Lecture 9
Question # 68
In the case of unassigned source and destination when subtracting and in the result ZF =1 OR CR=1 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST ? USRC

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4) : DEST > SRC
Correct Option : 3 From : Lecture 9

Question # 69
In the case of unassigned source and destination when subtracting and in the result ZF =0 AND CR=0 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST < USRC
4) : UDEST > USRC
Correct Option : 4 From : Lecture 9
Question # 70
In the case of unassigned source and destination when subtracting and in the result CR=0 then _____
1) : DEST = SRC
2) : DEST != SRC
3) : UDEST < USRC
4) : UDEST ? USRC
Correct Option : 4 From : Lecture 9
Question # 71
_____This jump is taken if the last arithmetic operation produced a zero in its destination. After a CMP it is taken if both operands were equal.
1) : Jump if zero(JZ)/Jump if equal(JE)
2) : Jump if equal(JE)
3) : Jump if zero(JZ)
4) : No Jump fot This
Correct Option : 1 From : Lecture 9
Question # 72
_____This jump is taken after a CMP if the unsigned source is smaller than or equal to the unsigned destination.
1) : JBE(Jump if not below or equal)
2) : JNA(Jump if not above)/JBE(Jump if not below or equal)
3) : JNA(Jump if not above)
4) : No Jump fot This
Correct Option : 2 From : Lecture 9
Question # 73
Numbers of any size can be added using a proper combination of _____.
1) : ADD and ADC
2) : ABD and ADC
3) : ADC and ADC
4) : None of the Given
Correct Option : 1 From : Lecture 11

Question # 74
Like addition with carry there is an instruction to subtract with borrows called_____.
1) : SwB
2) : SBB
3) : SBC
4) : SBBC
Correct Option : 2 From : Lecture 11

Question # 75
if “and ax, bx” instruction is given, There are _____ operations as a result

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1) : 16 AND
2) : 17 AND
3) : 32 AND
4) : 8 AND
Correct Option : 1 From : Lecture 12

Question # 76
_____can be used to check whether particular bits of a number are set or not.
1) : AND
2) : OR
3) : XOR
4) : NOT
Correct Option : 1 From : Lecture 12

Question # 77
_____can also be used as a masking operation to invert selective bits.
1) : AND
2) : OR
3) : XOR
4) : NOT
Correct Option : 3 From : Lecture 12

Question # 78
Masking Operations are Selective Bit _____
1) : Clearing, XOR, Inversion and Testing
2) : Clearing, Setting, Inversion and Testing
3) : Clearing, XOR, AND and Testing
4) : None of the Given
Correct Option : 2 From : Lecture 12

Question # 79
The _____ instruction allows temporary diversion and therefore reusability of code.
1) : CALL
2) : RET
3) : AND
4) : XOR
Correct Option : 1 From : Lecture 13

Question # 80
CALL takes a label as _____ and execution starts from that label,
1) : argument
2) : Lable
3) : TXt
4) : Register
Correct Option : 1 From : Lecture 13

Question # 81
When the _____instruction is encountered and it takes execution back to the instruction following the CALL.
1) : CALL
2) : RET
3) : AND
4) : XOR
Correct Option : 2 From : Lecture 13

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Question # 82
_____ Both the instructions are commonly used as a pair, however technically they are independent in their operation.
1) : RET and ADC
2) : Cal and SSb
3) : CALL and RET
4) : ADC and SSB
Correct Option : 3 From : Lecture 13

Question # 83
The CALL mechanism breaks the thread of execution and does not change registers, except _____.
1) : SI
2) : IP
3) : DI
4) : SP
Correct Option : 2 From : Lecture 13

Question # 84
Stack is a _____ that behaves in a first in last out manner.
1) : Program
2) : data structure
3) : Heap
4) : None of the Given
Correct Option : 2 From : Lecture 14

Question # 85
If _____ is not available, stack clearing by the callee is a complicated process.
1) : CALL
2) : SBB
3) : RET n
4) : None of the Given
Correct Option : 3 From : Lecture 14

Question # 86
When the stack will eventually become full, SP will reach 0, and thereafter wraparound producing unexpected results. This is called stack _____
1) : Overflow
2) : Leakage
3) : Error
4) : Pointer
Correct Option : 1 From : Lecture 14

Question # 87
The pop operation makes a copy from the top of the stack into its_____.
1) : Register
2) : operand
3) : RET n
4) : Pointer
Correct Option : 2 From : Lecture 14
Question # 88
_____decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack

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1) : PUSH
2) : POP
3) : CALL
4) : RET
Correct Option : 1 From : Lecture 14

Question # 89
POP transfers the word at the current top of stack (pointed to by SP) to the destination operand and then _____ SP by two to point to the new top of stack.
1) : increments
2) : dcrements
3) : ++
4) : --
Correct Option : 1 From : Lecture 14

Question # 90
The trick is to use the _____and _____operations and save the callers' value on the stack and recover it from there on return.
1) : POP, ADC
2) : CALL, RET
3) : CALL, RET n
4) : PUSH, POP
Correct Option : 4 From : Lecture 14
Question # 91
To access the arguments from the stack, the immediate idea that strikes is to _____ them off the stack.
1) : PUSH
2) : POP
3) : CALL
4) : Rrgister
Correct Option : 2 From : Lecture 15

Question # 92
push bp
we are _____
1) : sending bp copy to stack
2) : making bp copy from stack
3) : pushing bp on the stack
4) : doing nothing
Correct Option : 3 From : Lecture 15
Question # 93
Local Variables means variables that are used within the _____
1) : Subroutine
2) : Program
3) : CALL
4) : Label
Correct Option : 1 From : Lecture 15

Question # 94
Standard ASCII has 128 characters with assigned numbers from _____.
1) : 1to 129
2) : 0 to 127
3) : 0 to 128
4) : None of the Given
Correct Option : 2 From : Lecture 16

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Question # 95
When _____ is sent to the VGA card, it will turn pixels on and off in such a way that a visual representation of ‘A’ appears on the screen.
1) : 0x60
2) : 0x90
3) : 0x30
4) : 0x40
Correct Option : 4 From : Lecture 16

Question # 96
Which bit is refer to the Blinking of foreground character
1) : 6
2) : 7
3) : 5
4) : 3
Correct Option : 2 From : Lecture 16

Question # 97
Which bit is refer to the Intensity component of foreground color
1) : 4
2) : 5
3) : 3
4) : 7
Correct Option : 3 From : Lecture 16
Question # 98
Which bit is refer to the Green component of background color
1) : 1
2) : 5
3) : 3
4) : 7
Correct Option : 2 From : Lecture 16

Question # 99
Which bit is refer to the Green component of foreground color
1) : 1
2) : 5
3) : 3
4) : 7
Correct Option : 1 From : Lecture 16

Question # 100
String can be indicate bye given
1) : db 0x61, 0x61, 0x63
2) : db 'a', 'b', 'c'
3) : db 'abc'
4) : All of the above
Correct Option : 4 From : Lecture 16

Question # 101
The first form divides a 32bit number in DX:AX by its 16bit operand and stores the _____ quotient in AX
1) : 16bit
2) : 17bit
3) : 32bit

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4) : 64bit
Correct Option : 1 From : Lecture 17

Question # 102
The _____ (division) used in the process is integer division and not floating point division.
1) : DIV instruction
2) : ADC instruction
3) : SSB instruction
4) : DIVI instruction
Correct Option : 1 From : Lecture 17

Question # 103
_____(multiply) performs an unsigned multiplication of the source operand and the accumulator.
1) : Multi
2) : DIV
3) : MUL
4) : Move
Correct Option : 3 From : Lecture 18

Question # 104
The desired location on the screen can be calculated with the following formulae.
1) : location = (hypos * 80 + SP) * 3
2) : location = (hypos * 80 + slocation) * 2
3) : location = (hypos * 80 + epos) * 2
4) : None of the Given
Correct Option : 3 From : Lecture 18

Question # 105
To play with string there are 5 instructions that are _____
1) : STOS, LODS, CMPS, SCAS, and MOVS
2) : MUL, DIV, ADD, ADC and MOVE
3) : SSB, ADD, CMPS, ADC, and MOVS
4) : None of the Given
Correct Option : 1 From : Lecture 18
Question # 106
_____transfers a byte or word from register AL or AX to the string element addressed by ES:DI and updates DI to point to the next location.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 2 From : Lecture 18

Question # 107
_____ transfers a byte or word from the source location DS:SI to AL or AX and updates SI to point to the next location.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 1 From : Lecture 18
Question # 108

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_____compares a source byte or word in register AL or AX with the destination string element addressed by ES: DI and updates the flags.
1) : LODS
2) : STOS
3) : SCAS
4) : MOVE
Correct Option : 3 From : Lecture 18

Question # 109
_____ repeat the following string instruction while the zero flag is set and REPNE or REPNZ repeat the following instruction while the zero flag is not set.
1) : REP or REPZ
2) : REPE or REPZ
3) : REPE or RPZ
4) : RPE or REPZ
Correct Option : 2 From : Lecture 18
Question # 110
LES loads _____
1) : ES
2) : DS
3) : PS
4) : LS
Correct Option : 1 From : Lecture 20

Question # 111
LDS loads_____.
1) : ES
2) : DS
3) : PS
4) : LS
Correct Option : 2 From : Lecture 20

Question # 112
REP allows the instruction to be repeated _____ times allowing blocks of memory to be copied.
1) : DX
2) : CX
3) : BX
4) : AX
Correct Option : 2 From : Lecture 20

Question # 113
_____pops IP, then CS, and then FLAGS.
1) : Ret n
2) : REZA
3) : REPE
4) : IRET
Correct Option : 4 From : Lecture 21

Question # 114
_____ , Trap, Single step Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0

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Correct Option : 2 From : Lecture 21

Question # 115
_____,NMI-Non Maskable Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 3 From : Lecture 21

Question # 116
To hook an interrupt we change the _____ corresponding to that interrupt.
1) : SX
2) : vector
3) : AX
4) : BX
Correct Option : 2 From : Lecture 22
Question # 117
_____pops IP, then CS, and then FLAGS.
1) : Ret n
2) : REZA
3) : REPE
4) : IRET
Correct Option : 4 From : Lecture 21

Question #118
_____ , Trap, Single step Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 2 From : Lecture 21

Question #119
_____,NMI-Non Maskable Interrupt
1) : INT 0
2) : INT 1
3) : INT 3
4) : INT 0
Correct Option : 3 From : Lecture 21

Question # 120
To hook an interrupt we change the _____ corresponding to that interrupt.
1) : SX
2) : vector
3) : AX
4) : BX

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1. Assembly language is not a low level language.

a. True
b. False

2. In case of COM File first command parameter is stored at _____ offset of program segment prefix.
a. 0x80 (Not Confirm)
b. 0x82
c. 0x84
d. 0x86

3. Address always goes from
a. Processor to meory
b. Memory to processor
c. Memory to memory
d. None of the above

4. The sourse register in OUT is
a. AL or AX
b. BL or BX
c. CL or CX
d. DL or DX

5. By default CS is associated with
a. SS
b. BP
c. CX
d. IP

6. Which of the following pins of parallel port are grounded
a. 10-18
b. 18-25
c. 25-32
d. 32-39

7. In the instruction mov word [es:160], 0x1230, 30 represents the character
a. A
b. B
c. 0
d. 1

8. On executing 0x21 0x3D, if file cant be opened then
a. CF will contain 1
b. CF will contain 0
c. ZF will contain 1
d. ZF will contain 0

9. Which of the following IRQ is cascading interrupt
a. IRQ 0
b. IRQ 1
c. IRQ 2
d. IRQ 3

10. The execution of instruction mov word [es:160], 0x1230, will print a character on the screen at
a. First column of second row
b. Second column of first row

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c. Second column of second row
d. First column of third row

==========

1)))SHR and SAL are same?
.True (correct)
.False
2)))mov ax,0 will set ZF flag
.True
.False
3)))In 9 pin DB connector ,which pic is assigned to TD.
. 1
. 2
. 3(correct)
. 4
4)))Lower 16 bits of EAX are labeled as
. AX(correct)
. BX
.EAX
.none of above
5))) which is the special prefix used for repeating a block
.rep(correct)
.repeat
.repb
.repe
6)) JA can not after cmp if unsigned destinition is greater than source
.true
.false

Q=1

Conditional jump can only:

1. Far
2. short
3. near
4. all of the given

q=2:

Address is always go from:

1. Processor to memory

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2. Memory to processor
3. Memory to memory
4. None of given

Q=3;

Programmable interrupt controllers have two ports 20 and 21……port 20 is a control port while port 21 is ……..

1. The interrupt make register
2. Interrupt port
3. Output port
4. Input port

Q=4:

In the instruction “move word[es:160],0x1230 represent the charechter……

1. A
2. B
3. 0
4. 1

Q=5:

The 8088 processor divides interrupts into how many classes?

1. 2
2. 3
3. 4
4. 5

Q=6:

Which of the following is the pair of register used to access memory in string instruction?

1. DI and BP
2. SI and BP
3. DI and SI
4. DS and SI

Q=7:

In case of COM file,first command line parameter is stored at ……..offset of program segment prefix’

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1. 0x80
2. 0x82
3. 0x84
4. 0x86

Q=8:

The INT 0x13 service 0x03 is use to …

1. Read disk sector
2. Write disk sector
3. Reset disk sector
4. Get drive parameters

Q=9:

After the execution of STOSWB,the CX wil be……..

1. Incremented by 1
2. Incremented by 2
3. Decremented by 1
4. Decremented by 2

Q=10

The execution of the instruction “mov word [ES:160],0x1230”will print a character on the screen at:

1. First column of second row
2. Second column of first row
3. Second column of second row
4. First column of third row

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- **UNCATEGORIZED**
- **WHATEVER**

SATURDAY, 19 NOVEMBER 2011

CS401 Mid Term Solved

ADDED JAN 6, 2010, UNDER: CS401 MID TERM SOLVED

Question # 1

There are three busses to communicate the processor and memory named as _____

1) : address bus.,data bus and data bus.

2) : addressing bus.,data bus and data bus.

3) : address bus.,datamove bus and data bus.

4) : **address bus.,data bus and control bus..**

Correct Option : 4 From : Lecture 1

Question # 2

The address bus is unidirectional and address always travels from processor to memory.

1) : **TRUE**

2) : FALSE

3) :

4) :

Correct Option : 1 From : Lecture 1

Question # 3

Data bus is bidirectional because_____

1) : To way

2) : Data moves from both, processor to memory and memory to processor,

3) : **Data moves from both, processor to memory and memory to data Bus,**

4) : None of the Given

Correct Option : 3 From : Lecture 1

Question # 4

Control bus_____

1) : is Not Important.

2) : is Important .

3) : **bidirectional.**

4) : unidirectional .

Correct Option : 3 From : Lecture 1

Question # 5

A memory cell is an n-bit location to store data, normally _____also called a byte

1) : 4-bit

2) **: 8-bit**

3) : 6-bit

4) : 80-bit

Correct Option : 2 From : Lecture 1

Question # 6

The number of bits in a cell is called the cell width._____ define the memory completely.

1) : **Cell width and number of cells**,

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2) : cell number and width of the cells,
3) : width
4) : Height
Correct Option : 1 From : Lecture 1

Question # 7
for memory we define two dimensions. The first dimension defines how many _____bits are there in a single memory cell.
1**) : parallel**
2) : Vertical
3) : long
4) : short
Correct Option : 1 From : Lecture 1

Question # 8
_____ operation requires the same size of data bus and memory cell width.
1) : Normal
2**) : Best and simplest**
3) : first
4) : None of the Given
Correct Option : 2 From : Lecture 1

Question # 9
Control bus is only the mechanism. The responsibility of sending the appropriate signals on the control bus to the memory is of the_____.
1) : Data Bus
2**) : processor**
3) : Address Bus
4) : None of the Given
Correct Option : 2 From : Lecture 1

Question # 10
In "total: dw 0 " Opcode total is a _____
1) : Literal
2) : Variable
3) : **Label**
4) : Starting point
Correct Option : 3 From : Lecture 10

Question # 11
| 0 |-->| 1 | 1 | 0 | 1 | 0 | 0 | 0 | -->| C | is a example of _____
1) : Shl
2) : sar

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3) : Shr

4) : Sal

Correct Option : 3 From : Lecture 10

Question # 12

| C |‹--| 1 | 1 | 0 | 1 | 0 | 0 | 0 | ‹--| 0 | is a example of _____

1) : **Shl**

2) : sar

3) : Shr

4) : Sal

Correct Option : 1 From : Lecture 10

Question # 13

ADC has _____ operands.

1) : two

2) : **three**

3) : Five

4) : Zero

Correct Option : 2 From : Lecture 10

Question # 14

The basic purpose of a computer is to perform operations, and operations need _____.

1) : order

2) : nothing

3) **: operands**

4) : bit

Correct Option : 3 From : Lecture 2

Question # 15

Registers are like a scratch pad ram inside the processor and their operation is very much like normal _____.

1) : Number

2) : opreations

3) : **memory cells**

4) : None of the Given

Correct Option : 3 From : Lecture 2

Question # 16

There is a central register in every processor called the _____ and The word size of a processor is defined by the width of its_____.

1) : **accumulator,accumulator**

2) : data bus,accumulator

3) : accumulator, Address Bus

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4) : accumulator,memory
Correct Option : 1 From : Lecture 2

Question # 17
_____does not hold data but holds the address of data
1) : Pointer, Segment, or Base Register
2) : **Pointer, Index, or Base Register**
3) : General Registers
4) : Instruction Pointer
Correct Option : 2 From : Lecture 2

Question # 18
"The program counter holds the address of the next instruction to be _____"
1) **: executed.**
2) : called
3) : deleted
4) : copy
Correct Option : 1 From : Lecture 2

Question # 19
There are _____ types of "instruction groups"
1**) : 4**
2) : 5
3) : 3
4) : 2
Correct Option : 1 From : Lecture 2

Question # 20
These instructions are used to move data from one place to another.
1) : **TRUE**
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 2

Question # 21
"mov" instruction is related to the _____ *****.
1) : Arithmetic and Logic Instructions
2) : **Data Movement Instructions**
3) : Program Control Instructions
4) : Special Instructions
Correct Option : 2 From : Lecture 2

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Question # 22

_____allow changing specific processor behaviors and are used to play with it.

1) : **Special Instructions**

2) : Data Movement Instructions

3) : Program Control Instructions

4) : Arithmetic and Logic Instructions

Correct Option : 1 From : Lecture 2

Question # 23

8088 is a 16bit processor with its accumulator and all registers of _____.

1) : 32 bits

2) : 6 bits

3) : **16 bits**

4) : 64 bits

Correct Option : 3 From : Lecture 2

Question # 24

The _____ of a processor means the organization and functionalities of the registers it contains and the instructions that are valid on the processor.

1) : Manufactures

2) : **architecture**

3) : Deal

4) : None of the Given

Correct Option : 2 From : Lecture 2

Question # 25

Intel IAPX88 Architecture is _____

1) : **More then 25 old**

2) : New

3) : Not Good

4) : None of the Given

Correct Option : 1 From : Lecture 2

Question # 26

The iAPX88 architecture consists of_____registers.

1) : 13

2) : 12

3) : 9

4) : **14**

Correct Option : 4 From : Lecture 3

Question # 27

General Registers are _____

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1) : **AX, BX, CX, and DX**
2) : XA, BX, CX, and DX
3) : SS,SI and DI
4) : 3
Correct Option : 1 From : Lecture 3

Question # 28
AX means we are referring to the extended 16bit "A" register. Its upper and lower byte are separately accessible as _____.
1) : **AH and AL**
2) : A Lower and A Upper
3) : AL, AU
4) : AX
Correct Option : 1 From : Lecture 3

Question # 29
AX is General purpose Register where A stands for_____.
1) : Acadmic
2) : Ado
3) : Architecture
4) : **Accumulator**
Correct Option : 4 From : Lecture 3

Question # 30
The B of BX stands for _____because of its role in memory addressing.
1) : Busy
2) : **Base**
3) : Better
4) : None of the Given
Correct Option : 2 From : Lecture 3

Question # 31
The D of DX stands for Destination as it acts as the destination in _____.
1**) : I/O operations**
2) : operations
3) : memory cells
4) : Memory I/O operations
Correct Option : 1 From : Lecture 3

Question # 32
The C of CX stands for Counter as there are certain instructions that work with an automatic count in the _____.
1) : DI register

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2) : BX register
3) : **CX register**
4) : DX register
Correct Option : 3 From : Lecture 3

Question # 33
_____are the index registers of the Intel architecture which hold address of data and used in memory access.
1) : SI and SS
2) : PI and DI
3) : SI and IP
4) : **SI and DI**
Correct Option : 4 From : Lecture 3

Question # 34
In Intel IAPX88 architecture _____ is the special register containing the address of the next instruction to be executed.
1) : AX
2) : PI
3**) : IP**
4) : SI
Correct Option : 3 From : Lecture 3

Question # 35
SP is a memory pointer and is used indirectly by a set of _____.
1) **: instructions**
2) : Pointers
3) : Indexes
4) : Variables
Correct Option : 1 From : Lecture 3

Question # 36
_____is also a memory pointer containing the address in a special area of memory called the stack.
1) : SP
2) : BP
3) : PB
4) : AC
Correct Option : 2 From : Lecture 3

Question # 37
_____is bit wise significant and accordingly each bit is named separately.
1) : AX
2) : FS
3) : IP

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4) : **Flags Register**
Correct Option : 4 From : Lecture 3

Question # 38
When two 16bit numbers are added the answer can be 17 bits long, this extra bit that won't fit in the target register is placed in the _____where it can be used and tested
1) : carry flag
2) : Parity Flag
3) : Auxiliary Carry
4) : Zero Flag
Correct Option : 1 From : Lecture 3

Question # 39
Program is an ordered set of instructions for the processor.
1) : **TRUE**
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3

Question # 40
For Intel Architecture "operation destination, source" is way of writing things.
1) : TRUE
2) : FALSE
3) :
4) :
Correct Option : 1 From : Lecture 3

Question # 41
Operation code " add ax, bx " _____.
1) : Add the bx to ax and change the bx
2) : Add the ax to bx and change the ax
3) **: Add the bx to ax and change the ax**
4) : Add the bx to ax and change nothing
Correct Option : 3 From : Lecture 3

Question # 42
The maximum memory iAPX88 can access is_____.
1) : 1MB
2) : 2MB
3) : 3MB
4) : 128MB
Correct Option : 1 From : Lecture 4

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Question # 43

The maximum memory iAPX88 can access is 1MB which can be accessed with _____.

1) : 18 bits

2) : 20 bits

3) : 16 bits

4) : 2 bits

Correct Option : 2 From : Lecture 4

Question # 44

_____address of 1DED0 where the opcode B80500 is placed.

1) : **physical memory**

2) : memory

3) : efective

4) : None of the Given

Correct Option : 1 From : Lecture 4

Question # 45

16 bit of Segment and Offset Addresses can be converted to 20bit Address i.e

Segment Address with lower four bits zero + Offset Address with _____ four bits zero = 20bit Physical Address

1) : Middle

2) : lower

3) : Top

4) : **upper**

Correct Option : 4 From : Lecture 4

Question # 46

When adding two 20bit Addresses a carry if generated is dropped without being stored anywhere and the phenomenon is called address_____.

1) : **wraparound**

2) : mode

3) : ping

4) : error

Correct Option : 1 From : Lecture 4

Question # 47

segments can only be defined a 16byte boundaries called _____ boundaries.

1**) : segment**

2) : paragraph

3) : Cell

4) : RAM

Correct Option : 1 From : Lecture 4

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Question # 48

in a Program CS, DS, SS, and ES all had the same value in them. This is called _____.

1) : equel memory

2) : **overlapping segments**

3) : segments hidding

4) : overlapping SI

Correct Option : 2 From : Lecture 4

Question # 49

“db num1” size of the memory is _____

1) **: 1byte**

2) : 4bit

3) : 16bit

4) : 2byte

Correct Option : 1 From : Lecture 5

Question # 50

“ 1----------[org 0x0100]

2----------mov ax, [num1] ; load first number in ax

3----------mov bx, [num2] ; load second number in bx

4----------add ax, bx _____

5----------int 0x21

6----------

7----------num1: dw 5

8----------num2: dw 10

Comments for the 4 are :

1) : No comments Will be

2) : ; accumulate sum in add

3) : ; accumulate sum in ax

4) : ; accumulate sum in Bx

Correct Option : 3 From : Lecture 5

Question # 51

In “ mov ax, bx ” is _____ Addressing Modes.

1) : Immediate

2) : Indirect

3) : Direct

4) : **Register**

Correct Option : 4 From : Lecture 5

Question # 52

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In “mov ax, [bx] ” is _____ Addressing Modes

1) : **Based Register Indirect**

2) : Indirect

3) : Base Indirect

4) : Immediate

Correct Option : 1 From : Lecture 5

Question # 53

In “mov ax, 5 ” is _____ Addressing Modes

1) : **Immediate**

2) : Indirect

3) : Indirect

4) : Register

Correct Option : 1 From : Lecture 6

Question # 54

In “ mov ax, [num1+bx] ” is _____ ADDRESSING

1) : OFFSET+ Indirect

2) : Register + Direct

3) : Indirect + Reference

4) : **BASEd REGISTER + OFFSET**

Correct Option : 4 From : Lecture 7

Question # 55

“base + offset addressing ” gives This number which came as the result of addition is called the _____.

1) : Address

2) : mode

3) : **effective address**

4) : Physical Address

Correct Option : 3 From : Lecture 7

Question # 56

“mov ax, [cs:bx]” associates _____ for this one instruction

1) : CS with BX

2) : **BX with CS**

3) : BX with AX

4) : None of the Given

Correct Option : 2 From : Lecture 7

Question # 57

For example

BX=0100

DS=FFF0

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And Opcode are;
move [bx+0x0100], Ax
now what is the effective memory address;
1) : 0020
2) : 0200
3) : 0300
4) : 0x02
Correct Option : 2 From : Lecture 7

Question # 59
In " mov [1234], al " is _____ Addressing Modes.
1) : Immediate
2) : Indirect
3) : Direct
4) : Register
Correct Option : 3 From : Lecture 8

Question # 60
In " mov [SI], AX " is _____ Addressing Modes.
1) : Basef Register Indirect
2) : Indirect
3) : **Indexed Register Indirect**
4) : Immediate
Correct Option : 3 From : Lecture 8

Question # 61
In " mov ax, [bx - Si] " is _____ ADDRESSING
1) : Basef Register Indirect
2) : Indirect
3) : Direct
4) : **illegal**
Correct Option : 4 From : Lecture 8

Question # 62
In " mov ax, [BL] " there is error i.e. _____
1) : Address must be 16bit
2) : Address must be 8bit
3) : Address must be 4bit
4) : 8 bit to 16 bit move illegal
Correct Option : 4 From : Lecture 8

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Question # 63

In " mov ax, [SI+DI] " there is error i.e. _____

1) **: Two indexes can't use as Memory Address**

2) : index can't use as Memory Address

3) : I don't Know

4) : None of the Given

Correct Option : 1 From : Lecture 8

Question # 64

In JNE and JNZ there is difference for only _____;

1) **: Programmer or Logic**

2) : Assembler

3) : Debugger

4) : IAPX88

Correct Option : 1 From : Lecture 9

Question # 65

JMP is Instruction that on executing take jump regardless of the state of all flags is called_____

1) : Jump

2) : Conditional jump

3) : **Unconditional jump**

4) : Stay

Correct Option : 3 From : Lecture 9

Question # 66

When result of the source subtraction from the destination is zero, zero flag is set i.e. ZF=1

its mean that;

1**) : DEST = SRC**

2) : DEST != SRC

3) : DEST < SRC

4) : DEST > SRC

Correct Option : 1 From : Lecture 9

Question # 67

When an unsigned source is subtracted from an unsigned destination and the destination is smaller, borrow is needed which sets the _____.

1) : carry flag i.e CF = 0

2) : **carry flag i.e CF = 1**

3) : Carry Flag + ZF=1

4) : None of the Given

Correct Option : 2 From : Lecture 9

Question # 68

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In the case of unassigned source and destination when subtracting and in the result ZF =1 OR CR=1 then _____

1) : DEST = SRC

2) : DEST != SRC

3) : **UDEST ? USRC**

4) : DEST > SRC

Correct Option : 3 From : Lecture 9

Question # 69

In the case of unassigned source and destination when subtracting and in the result ZF =0 AND CR=0 then _____

1) : DEST = SRC

2) : DEST != SRC

3) : UDEST < USRC

4) : UDEST > USRC

Correct Option : 4 From : Lecture 9

Question # 70

In the case of unassigned source and destination when subtracting and in the result CR=0 then _____

1) : DEST = SRC

2) : DEST != SRC

3) : UDEST < USRC

4) **: UDEST ? USRC**

Correct Option : 4 From : Lecture 9

Question # 71

_____This jump is taken if the last arithmetic operation produced a zero in its destination. After a CMP it is taken if both operands were equal.

1) **: Jump if zero(JZ)/Jump if equal(JE)**

2) : Jump if equal(JE)

3) : Jump if zero(JZ)

4) : No Jump fot This

Correct Option : 1 From : Lecture 9

Question # 72

_____This jump is taken after a CMP if the unsigned source is smaller than or equal to the unsigned destination.

1) : JBE(Jump if not below or equal)

2) : **JNA(Jump if not above)/JBE(Jump if not below or equal)**

3) : JNA(Jump if not above)

4) : No Jump fot This

Correct Option : 2 From : Lecture 9

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CS401 Computer Architecture and Assembly Language Programming Quiz No 1 Solution and Discussion Spring 2014 Due Date: May 08, 2014

Posted by + M.Tariq Malik on April 26, 2014 at 9:57am in CS401 Computer Architecture and Assembly Language ProgrammingBack to CS401 Computer Architecture and Assembly Language Programming Discussions

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Permalink Reply by ĴĮÃ ČĤ on April 26, 2014 at 11:39am

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Permalink Reply by abira ali on May 7, 2014 at 2:26pm

Question # 2

Instruction Pointer holds the address of the

Previous instruction to be executed

Current instruction

Next instruction to be executed

None of the given

Question # 3 of 10

Register whose each bit specify a different meaning is

Accumulator Register vuzs

Pointer Register

Index register

Flag register

Question # 4 of 10

Bydefault CS is associated with

SS

BP

CX

IP

Question # 5 of 10

Memory to Memory operation is allowed

True

False

Question # 6 of 10

Size Mismatch Error is a syntax error

False (Size mismatch is logical error)

True

Question # 7 of 10

unconditional jump can be

near

short

far

all of the given

Question # 8 of 10

Register are storage cell

Outside the processor

Both inside and outside the processor

Inside the processor

None of the given

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Question # 9 of 10

Register to Register Operation is not allowed

True

False

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The operation of CMP is to Subtract source from destination

True

False

Size Mismatch Error is a syntax error

False

True

Unconditional jump

Execute in every condition whether true or false

If the condition is true

If the condition is false

None of the given

Which type of Rotation it is "Every bit moves one position to the right and the bit dropped from the right is inserted at the eft. This bit is also copied into the carry flag."

ROL

RCR

RCL

None of the given

Assembly languague is not a low level language.

true

False

In JA jump is not taken after a CMP if the unsigned destination is larger than the unsigned source.

True

False

Group of bits processor uses to inform memory which element to read/write is collectively known as

Control bus

Data bus

Address bus

RAM

Memory to Memory operation is allowed

True

False

90 is the op-code of

Do nothing

Add

Subtract

Multiplication

we can not add two base register i.e. (bx+bp) or cant use in an instruction

True

False

Intel follow

Littel endian

Big endian

Both littel endian and big endian

None of the given

SHL and SAL are same

True

False

The first 16-bit processor produced by "Intel" was 8085

True

False

The first 16-bit processor produced by "Intel" was 8085

True

False

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The extension of assembly languague file is

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When a large number is subtracted from a smaller number, a borrow is needed; in this case which flag will be set

ZF

CF

SF

OF

All the addressing mechanisms in iAPX88 return a number called _____ address.

Effective address

Physical address

Direct address

None of the given

Which type of shifting is "Inserts a zero from the left and moves every bit one position to the right and copies the rightmost bit in the carry flag."

SHL

SAL

SAR

None of the given

mov [1234],ax is an example of

Direct addressing

Base register indirect

Base+index

None of the given

Registers are also called scratch pad ram

True

False

The basic function of register is to?

Hold the operand

Hold the operator

Hold both the operator and operand

None of the given

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The jump is taken if the last arithmetic operation changed the sign unexpectedly.

JO

JNO

JNZ

JZ

In JA jump is not taken after a CMP if the unsigned destination is larger than the unsigned source.

True

False

which type of rotation it is "The carry flag is inserted from the left, every bit moves one position to the right, and the right most bit is dropped in the carry flag. "

RCR

ROL

RCL

ROR

which type of rotation it is "The carry flag is inserted from the left, every bit moves one position to the right, and the right most bit is dropped in the carry flag. "

RCR

ROL

RCL

ROR

This jump is taken if the last arithmetic operation produced a number in its destination that has even parity , Which jump is taken

JP

JPE

JNP

both JP and JPE

In direct addressing the memory address given in the instruction is

When a large number is subtracted from a smaller number, a borrow is needed; in this case which flag will be set

ZF

CF

SF

OF

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SHL and SAL are same

True

False

we can not Subrtace index register from the base register(bx-si)in assemlby language vuzs

True

False

Group of bits processor uses to inform memory which element to read/write is collectively known as

Control bus

Data bus

Address bus

RAM

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Permalink Reply by + Mărιε Яɑjpuт + on May 7, 2014 at 5:12pm

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Permalink Reply by cancerian on May 7, 2014 at 8:30pm

8 chapters cover 22 lectures. I observed that first four lectures cover first chapter so please give the breakup of other eight chapters like

Chapter # 1 (lectures # 1,2,3,4)

Chapter #. 2 (?)

Chapter # 3

Chapter #. 4

Chapter #5

Chapter # 6

Chapter # 7

Chapter # 8

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Permalink Reply by + ✿´´ᴄᴍ(ɴɪsɑ)``✿ on May 8, 2014 at 1:23pm

10 marks ka quiz hai +Mărіє Яɑjрuт+

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Permalink Reply by + M.Tariq Malik on May 7, 2014 at 10:40pm

Question # 1 of 10 (Start time: 12:57:07 PM) Total Marks: 1

Mechanism used to drop carry for making the calculated address valid is known as:

Select correct option:

Carry Overload

Overflow

Address Wraparound

None of the above

Question # 2 of 10 (Start time: 12:58:36 PM) Total Marks: 1

we can not Subrtace index register from the base register(bx-si)in assemlby language

Select correct option:

True

False

Question # 3 of 10 (Start time: 12:59:56 PM) Total Marks: 1

Physical address calculation depends on

Select correct option:

Base address

Effective address

Offset Address

None of the above

Question # 4 of 10 (Start time: 01:01:14 PM) Total Marks: 1

Simple CMP instruction uses _____ operation

Select correct option:

Addition

Division

Subtraction

Multiplicaion

Question # 5 of 10 (Start time: 01:02:45 PM) Total Marks: 1

SS is by defult associated with

Select correct option:

BP

IP

SP

BP

Question # 6 of 10 (Start time: 01:04:14 PM) Total Marks: 1

When a 32 bit number is divided by a 16 bit number, the remainder is of

Select correct option:

4 bits

8 bits

16 bits

32 bits

Question # 7 of 10 (Start time: 03:53:38 PM) Total Marks: 1

Which of the following is not a valid instruction in assembly language?

Select correct option:

MOV AX, 55

MOV AX, BX

MOV CS, 0xb800

MOV BX, AX

Question # 8 of 10 (Start time: 03:55:09 PM) Total Marks: 1

Memory to Memory operation is allowed

Select correct option:

True

False

The other directive is “define word” or “dw” with the same syntax as “db” but reserving a whole word of __ bits instead of a byte.

Select correct option:

32

8

16

64

Question # 10 of 10 (Start time: 03:58:10 PM) Total Marks: 1

we can not add two base register i.e. (bx+bp) or cant use in an instruction

Select correct option:

True

False

BR,

Answers:

1) Address Wraparound

2) True

3) Effective address

4) Subtaction

5) BP

6) 16 bits

7) MOV CS, 0xb800

8) False

9) 8 bits

10) True>

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2aqlargmrfxmzPermalink Reply by 2aqlargmrfxmz on May 7, 2014 at 11:11pm

Tariq Bhai question No 9 ka ans 8 bits nai 16 bits ha

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Permalink Reply by + ✿´´ᴄᴍ(ɴɪsɑ)``✿ on May 8, 2014 at 1:25pm

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1quypvq75nb4qPermalink Reply by 1quypvq75nb4q on May 8, 2014 at 4:28pm

Today main chat room ma ya quiz solved kiya tha sub nay ??? ager koi ans theek nai ha to correct ker den..thax

1. When a large number is subtracted from a smaller number, a borrow is needed; in this case which flag will be se

cf

2. jump is not position relative but is absolute

far

3. Group of bits processor uses to inform memory which element to read/write is collectively known as

address bus

4. A complete _____ is called a pass over the array

ITTERATION

5. There are _____ types of address wraparound

2

6. All the addressing mechanisms in iAPX88 return a number called _____ address.

Effective

7. Whenever we need access to a memory location whose address is not known until run-time we use _____.

INDEX REGISTOR

8. DX plays an important role in arithmetic _____.

DIVISION

9. If BL contains 00000101 then after a Single Right Shift, BL will contain

00000011

10. To multiply a number in a register by 2 the number is _____.

Shifted right one bit

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1quypvq75nb4qPermalink Reply by 1quypvq75nb4q on May 8, 2014 at 6:13pm

SP is associated (by default) with _____.

cs

Intel follows _____.

Little endian

The maximum amount of memory accessible using 8085 processor is _____.

64 kb

Which of the following addressing scheme has been used in the instruction MOV [BX], AX?.....

base register direct access

Instruction Pointer holds the address of the.....

next instruction to b executd

Sending the appropriate signals on the control bus to the memory is the responsibility of _____.

processor conferm

Register whose each bit specify a different meaning is--------

flag Register

The iAPX88 processor supports _____modes of memory access.

7

CX register is mostly used as a

counter conferm

Constant can never be used as _____.

source

destination

both source and destination

immediate source

Which one of the following is an illegal instruction?

MOV ax,[bx+bp]

In _____ every bit moves one position to the right and the bit dropped from the right is inserted at the left and also copied into the carry flag ?

RCR

RCL

ROR

ROL

In _____ operation, a carry flag is inserted from the left moving every bit one position to the right, with the right most bit is dropped in the carry flag".

RCR

ROL

RCL

ROR

Which of the following is not a valid instruction in assembly language?

MOV CS, 0xb800

Data bus is _____.

bidirectional conferm

Simple CMP instruction uses _____ operation.

Subtraction

The _____ operation is about shifting every bit one place to the right with a copy of the most significant bit left at the most significant place. The bit dropped from the right is caught in the carry basket.

Shift Logical Right (SHR)

Shift Arithmetic Right (SAR)

Shift Arithmetic Left (SAL)

Shift Logical Left (SHL)

After the execution of SAR instruction, _____.

The msb is replaced by a 0

The msb retains its original value

The msb is replaced by 1

The msb is replaced by the value of CF

Which of the following instruction is effectively same as to multiply the value of AX by 8?

MUL AX, 3

The shift logical left operation is the exact _____ of shift logical right.

oposite

The _____ operation is about shifting every bit one place to the right with a copy of the most significant bit left at the most significant place. The bit dropped from the right is caught in the carry basket.

Shift Logical Left (SHL)

SHR

SHL

The basic function of register is to

Hold the operand

When a 32 bit number is divided by a 16 bit number, the remainder is of

8

---

n _____ every bit moves one position to the right and the bit dropped from the right is inserted at the left and also copied into the carry flag ?

ROL

RCR

RCL

ROR

---

mov [bp], al" moves the one byte contents of the AL register to the address contained in BP register in the current _____.

Stack Segment

Data Segment

Code Segment

Extra SegmentExtra Segment

Which of the following shift operation inserts a zero from the left and moves every bit one position to the right and copies the rightmost bit in the carry flag ?

SHL

In case of short jump, the offset is stored in _____ .

1 2 4 16 bytes?

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1quypvq75nb4qPermalink Reply by 1quypvq75nb4q on May 8, 2014 at 7:58pm

The _____ operation is about shifting every bit one place to the right with a copy of the most significant bit left at the most significant place. The bit dropped from the right is caught in the carry basket.

Shift Logical Right (SHR)

Shift Arithmetic Right (SAR)

Shift Arithmetic Left (SAL)

Shift Logical Left (SHL)

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In Left - Shift - Operation , the left most bit _____
Select correct option
will be dropped
will go into CF
will be moved to the right - most position
will always be 1
Question # 2 of 10 (Start time: 09 :16 :53 PM) Total Marks: 1
" mov [bp] , al " moves the one byte contents of the AL register to the address contained in BP register in the current _____ .
Select correct option :
Stack Segment
Data Segment
Code Segment
Extra Segment
Question # 3 of 10 (Start time: 09 :17 :33 PM) Total Marks: 1
CX register is mostly used as a
Select correct option :
counter register
flag register
base register
desination register
Question # 4 of 10 (Start time: 09 :18 :55 PM) Total Marks: 1
By default CS is associated with
Select correct option :
SS
BP
CX
IP
Question # 5 of 10 (Start time: 09 :20 :30 PM) Total Marks: 1
Which of the following shift operation inserts a zero from the left and moves every bit one position to the right and copies the rightmost bit in the carry flag ?
Select correct option :
SHL
SAL

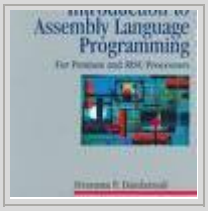
SONU MUGHAL

SAR
SHR
Question # 6 of 10 (Start time:
09 :21 :58 PM) Total Marks: 1
The _____ operation is about shifting every bit one place to the right with a copy of the most significant bit left at the most significant place . The bit dropped from the right is caught in the carry basket .
Select correct option :
Shift Logical Left (SHL)
Shift Logical Right (SHR)
Shift Arithmetic (SAR)
Shift Arithmetic Left (SAL)
Question # 7 of 10 (Start time:
09 :23 :17 PM) Total Marks: 1
In _____ every bit moves one position to the right and the bit dropped from the right is inserted at the left and also copied into the carry flag ?
Select correct option :
ROL
RCR
RCL
ROR
Question # 8 of 10 (Start time:
09 :24 :15 PM) Total Marks: 1
Which one of the following is an illegal instruction?
Select correct option
MOV AX ,BX
MOV AX ,65
MOV ax ,[bx + bp]
Mov BX , 10
Question # 9 of 10 (Start time:
09 :24 :54 PM) Total Marks: 1
The shift logical left operation is the exact _____ of shift logical right .
Select correct option :
Similar
Opposite
implementation
comparison
Question # 10 of 10 (Start time :
09 :25 :41 PM) Total Marks: 1
Physical address calculation depends on

UNU MUGHAL

Select correct option :
Base address
Effective address
Offset Address
Segment Address

1



CS401 Computer Architecture and Assembly Language Programming

2020 members

Description

Comments Discussions **Members**



CS401 Online Quiz No 02 Solution & Discussion Last Date:17-12-2014

by + M.Tariq Malik

Dec 8, 2014

CS401 Online Quiz No 02 Solution & Discussion Last Date:17-12-2014

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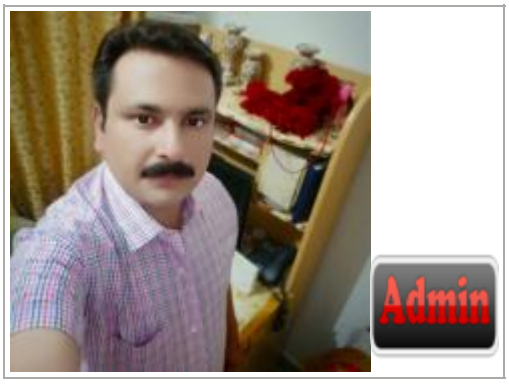
Dear Students

This is to inform that quiz 02 will be opened on 16th December, 2014 and last date to attempt quiz will be 17th December, 2014.

Instructions:

- You can start attempting the quiz at any time but within given date(s) by clicking the quick link for Quiz on VU-LMS as it will become enabled within the mentioned dates. As soon as the time will be over, it will automatically be disabled and will not be available to attempt it.

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+ M.Tariq Malik

CS401 Quiz 2

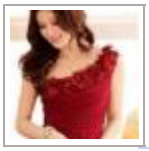
Dec 17, 2014

- 

nina

XOR can also be used as a _____ to invert selective bits.
Making operations

Dec 17, 2014

- 

Syeda Shahzadi Bukhari (BS 8th)

Question # 1 of 10 (Start time: 09:38:11 PM) Total Marks: 1
In case of near jump, the relative address is stored in _____ bits.
Select correct option:

4
8
16 .....right
32

Question # 2 of 10 (Start time: 09:38:39 PM) Total Marks: 1
The Jump command that does not depend on FLAG register is
Select correct option:

JCXZ
JO
JNE.....right
JP

Question # 3 of 10 (Start time: 09:40:04 PM) Total Marks: 1
In SCAS Example, We use SCASB with _____ and a zero in AL register to find a zero byte in a string.
Select correct option:

REPNE ...right
SCAS
MOV
CALL

Question # 4 of 10 (Start time: 09:40:24 PM) Total Marks: 1
How much byte/bytes cannot be pushed and popped from the stack at once.
Select correct option:

Single
Double
Three ....right not sure
Four

Question # 5 of 10 (Start time: 09:41:55 PM) Total Marks: 1
Which of the following are the two variants of STOS instruction?
Select correct option:

STOSB and STOSW .....right
STOS and STOSES
STOS1 and STOS2
STOSA and STOSB

Question # 6 of 10 (Start time: 09:43:00 PM) Total Marks: 1
____ jump is not position relative but is absolute
Select correct option:

Near
Short
Far ....right
Extra

Question # 7 of 10 (Start time: 09:43:22 PM) Total Marks: 1
DW can store _____ bit value in it.
Select correct option:

8
16
24
32 ..right

Question # 8 of 10 (Start time: 09:44:13 PM) Total Marks: 1
LDS instruction loads ____ register.
Select correct option:

ES
DS .....right
CX

Question # 9 of 10 (Start time: 09:44:46 PM) Total Marks: 1
Our computers screen is like a 2-D array having _____ rows and _____ columns.
Select correct option:

25, 40
25, 80
80, 25 .....right

Question # 10 of 10 (Start time: 09:46:08 PM) Total Marks: 1
To convert the case of a character, we add or subtract _____ from its ASCII code.
Select correct option:

0x10
0x20.....right
0x30
0x41

Dec 17, 2014

1 member likes this

4



ALL CS401 solved Quiz no 1 and 2 (2013 and 2014) in one discussion

by + WASI(S.Admin) +
May 27, 2014

Cs 401 Quiz no 1 (2014)@ wasi

Question # 1 of 10 (Start time: 12:57:07 PM) Total Marks: 1
Mechanism used to drop carry for making the calculated address valid is known as:
Select correct option:
Carry Overload
Overflow
Address Wraparound
None of the above

Question # 2 of 10 (Start time: 12:58:36 PM) Total Marks: 1
we can not Subrtace index register from the base register(bx-si)in assemlby language
Select correct option:
True
False

Question # 3 of 10 (Start time: 12:59:56 PM) Total Marks: 1
Physical address calculation depends on
Select correct option:
Base address
Effective address
Offset Address
None of the above

Question # 4 of 10 (Start time: 01:01:14 PM) Total Marks: 1
Simple CMP instruction uses _____ operation
Select correct option:
Addition
Division
Subtraction
Multiplicaion

Question # 5 of 10 (Start time: 01:02:45 PM) Total Marks: 1
SS is by defult associated with
Select correct option:
BP
IP
SP
BP

Question # 6 of 10 (Start time: 01:04:14 PM) Total Marks: 1
When a 32 bit number is divided by a 16 bit number, the remainder is of
Select correct option:
4 bits
8 bits
16 bits
32 bits

Question # 7 of 10 (Start time: 03:53:38 PM) Total Marks: 1
Which of the following is not a valid instruction in assembly language?
Select correct option:
MOV AX, 55
MOV AX, BX
MOV CS, 0xb800
MOV BX, AX

Question # 8 of 10 (Start time: 03:55:09 PM) Total Marks: 1
Memory to Memory operation is allowed
Select correct option:
True
False

Question # 9 of 10 The other directive is “define word” or “dw” with the same syntax as “db” but reserving a whole word of __ bits instead of a byte.
Select correct option:
32
8
16
64

Question # 10 of 10 (Start time: 03:58:10 PM) Total Marks: 1
we can not add two base register i.e. (bx+bp) or cant use in an instruction
Select correct option:

True
False



+ WASI(S.Admin) +

Cs 401 Quiz no 1 (2014)@ wasi

Question # 1 of 10 (Start time: 12:57:07 PM) Total Marks: 1
Mechanism used to drop carry for making the calculated address valid is known as:
Select correct option:
Carry Overload
Overflow
Address Wraparound
None of the above

Question # 2 of 10 (Start time: 12:58:36 PM) Total Marks: 1
we can not Subrtace index register from the base register(bx-si)in assemlby language
Select correct option:
True
False

Question # 3 of 10 (Start time: 12:59:56 PM) Total Marks: 1
Physical address calculation depends on
Select correct option:
Base address
Effective address
Offset Address
None of the above

Question # 4 of 10 (Start time: 01:01:14 PM) Total Marks: 1
Simple CMP instruction uses _____ operation
Select correct option:
Addition
Division
Subtraction
Multiplicaion

Question # 5 of 10 (Start time: 01:02:45 PM) Total Marks: 1
SS is by defult associated with
Select correct option:
BP
IP
SP
BP

Question # 6 of 10 (Start time: 01:04:14 PM) Total Marks: 1
When a 32 bit number is divided by a 16 bit number, the remainder is of
Select correct option:
4 bits
8 bits
16 bits
32 bits

Question # 7 of 10 (Start time: 03:53:38 PM) Total Marks: 1
Which of the following is not a valid instruction in assembly language?
Select correct option:
MOV AX, 55
MOV AX, BX
MOV CS, 0xb800
MOV BX, AX

Question # 8 of 10 (Start time: 03:55:09 PM) Total Marks: 1
Memory to Memory operation is allowed
Select correct option:
True
False

Question # 9 of 10 The other directive is “define word” or “dw” with the same syntax as “db” but reserving a whole word of __ bits instead of a byte.
Select correct option:

32
8
16
64

Question # 10 of 10 (Start time: 03:58:10 PM) Total Marks: 1
we can not add two base register i.e. (bx+bp) or cant use in an instruction
Select correct option:
True
False

Cs 401 Quiz no 1 (2014)@ wasi

1. When a large number is subtracted from a smaller number, a borrow is needed; in this case which flag will be
Ans cf

2. jump is not position relative but is absolute.

Ans far

3. Group of bits processor uses to inform memory which element to read/write is collectively known as.

Ans address bus

4. A complete _____ is called a pass over the array.

Ans ITTERATION

5. There are _____ types of address wraparound.

Ans 2

6. All the addressing mechanisms in iAPX88 return a number called _____ address.

Ans Effective

7. Whenever we need access to a memory location whose address is not known until run-time we use _____.

Ans INDEX REGISTOR

8. DX plays an important role in arithmetic _____.

Ans DIVISION

9. If BL contains 00000101 then after a Single Right Shift, BL will contain

Ans 00000011

10. To multiply a number in a register by 2 the number is _____.

Ans Shifted right one bit

11. SP is associated (by default) with _____.

Ans cs

12. Intel follows _____.

Ans Little endian

13 The maximum amount of memory accessible using 8085 processor is _____.

Ans 64 kb

14. Which of the following addressing scheme has been used in the instruction MOV [BX], AX?.....

Ans base register direct access

15.Instruction Pointer holds the address of the.....

Ans next instruction to b executd

16.Sending the appropriate signals on the control bus to the memory is the responsibility of _____.

Ans processor conferm

17. Register whose each bit specify a different meaning is--------

Ans flag Register

18. The iAPX88 processor supports _____modes of memory access.
Ans 7

19. CX register is mostly used as a
Ans counter conferm

20.Which one of the following is an illegal instruction?
Ans MOV ax,[bx+bp]

21. Which of the following is not a valid instruction in assembly language?
Ans MOV CS, 0xb800

22. Data bus is _____.
Ans bidirectional conferm

23.Simple CMP instruction uses _____ operation.

Ans Subtraction

24. Which of the following instruction is effectively same as to multiply the value of AX by 8?
Ans MUL AX, 3

25. The shift logical left operation is the exact _____ of shift logical right.

Ans oposite

26. When a 32 bit number is divided by a 16 bit number, the remainder is of
Ans 8

27. Which of the following shift operation inserts a zero from the left and moves every bit one position to the right and copies the rightmost bit in the carry flag ?
Ans SHL

28.In _____ every bit moves one position to the right and the bit dropped from the right is inserted at the left and also copied into the carry flag ?
RCR

RCL

Ans ROR

ROL

29. In _____ operation, a carry flag is inserted from the left moving every bit one position to the right, with the right most bit is dropped in the carry flag".

Ans RCR

ROL

RCL

ROR

4

Both DS and ES can be used to access the video memory. However we commonly keep DS for accessing our data, and load ES with the segment of video memory.
Select correct option:

True

False

PAGE 81

Question # 2 of 10 (Start time: 03:17:23 PM) Total Marks: 1
How many characters standard ASCII has?
Select correct option:

512

256

128

64

During the CALL operation, the current value of the instruction pointer is automatically saved on the stack, and the destination of CALL is loaded in the instruction pointer.
Select correct option:

True
False

VGA stands for
Select correct option:

Video Graphic Accumulator
Video Graphics Adapter
Visual Graphics Adapter
Video Graphics Application

Video Graphics Adapter

_____ transfers the word at the current top of stack (pointed to by SP) to the destination operand and then increments SP by two to point to the new top of stack.
Select correct option:

PUSH
POP
CALL
None of the given

The execution of the instruction "mov word [ES : 160], 0x1230" will print a character on the screen at:
Select correct option:

First column of second row
Second column of first row
Second column of second row
First column of third row

The Operation of pop ax is AX <-- [SP] SP <-- SP-2
Select correct option:

True
False

_____ function decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.
Select correct option:

POP
PUSH
RET
ADD

Far calls are called intra segment calls.
Select correct option:

True
False

STOS is often used to clear a block of memory or fill it with a constant.
Select correct option:

True
False

How many characters were defined by standard ASCII?

Select correct option:

132

124

122

128

Stack clearing by the caller needs an extra instruction on behalf of the caller after every call made to the subroutine, unnecessarily increasing instructions in the program.
Select correct option:

True
False

The direction of movement is controlled with the _____in the flags register. If this flag is cleared the direction is from lower addresses towards higher addresses and if this flag is set the direction

is from higher addresses to lower addresses.
Select correct option:

Direction Flag (DF)
Control Flag (CF)
Carry Flag (CF)
Non of above

ASCII stands for_____.
Select correct option:

American Standard Code for Information Interaction
American Standard Code for Information Interchange
American Standard Communication for Integer Interchange
American Scientific Communication for Integer Interaction

During the CALL operation, the current value of the instruction pointer is automatically saved on the stack, and the destination of CALL is loaded in the instruction pointer.
Select correct option:

Extended ASCII has 256 characters with assigned numbers from
Select correct option:

1 to 255
0 to 256
0 to 255
1 to 256

Hexadecimal is the prevalent and standard format for representation of characters in computers.
Select correct option:

True
False

The execution of the instruction "mov word [ES : 160], 0x1230" will print a character on the screen at:
Select correct option:

First column of second row
Second column of first row
Second column of second row
First column of third row

In the instruction "mov word [es:160], 0x1230", 12 means:
Select correct option:

green color on black background
green color on blue background
black color on green background
blue color on green background

This top of stack is contained in the ____ register.
Select correct option:

SP
BP
AX
BX

PUSH increments SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.
Select correct option:

True
False

Page 71

The reduction in code size and the improvement in speed are the two reasons why block processing instructions were introduced in the _____ processor.
Select correct option:

8088
8085
8080
iAPX386

MOVS is used to _____ a block of memory.
Select correct option:

Save
Move

Delete
Push

The operation of PUSH is not similar to CALL however with a register other than the instruction pointer.
Select correct option:

True
False

Reference: operation of PUSH is similar to CALL however with a register other than the instruction pointer. page 69

Both DS and ES can be used to access the video memory. However we commonly keep DS for accessing our data, and load ES with the segment of video memory.
Select correct option:

True
False

Which bit of the attributes byte represents the blue component of foreground color ?
Select correct option:

0
1
2
3

SCAS compares a source byte or word in register AL or AX with the _____string element addressed by ES: DI and updates the flags.

Source

Destination

Flag

Register

page 92

An element is pushed on the stack SP is decremented by ____ as the 8088 stack works on word sized elements.

Three

two

four

five

page 68

To access the arguments from the stack, the immediate idea that strikes is to ____them off the stack.

push

pop

add

insert

We use _____ to access the parameters that are stay on the stack with out popping them.

pop

DS not sure

PUSH

BP

How many characters were defined by standard ASCII?

132

124

128

ASCII table is the contiguous arrangement of the uppercase alphabets (41-5A), the lowercase alphabets (61-7A), and the numbers _____

31-40

29-39

30-39

page no 80

The purpose of MOVS instruction is to move a memory location to register

True

False

_____ decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.

push

pop

call

None

This top of stack is contained in the ____ register.

SP

BP

AX

To access the arguments from the stack, the immediate idea that strikes is to ____them off the stack.
Select correct option:
Push
Pop
Add
Insert

Parameters clears from the stack by the
Select correct option:
caller
callee
caller and callee
None of the given

There are just____ block processing instructions in 8088.

Select correct option:
6
5
4
3

_____ decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.
Select correct option:
PUSH
POP
CALL
None of the Above

The operation of PUSH is not similar to CALL however with a register other than the instruction pointer.
Select correct option:
True
False

The direction of movement is controlled with the _____in the flags register. If this flag is cleared the direction is from lower addresses towards higher addresses and if this flag is set the direction is from higher addresses to lower addresses.
Select correct option:
Direction Flag (DF)
Control Flag (CF)
Carry Flag (CF)
Non of above

Hexadecimal is the prevalent and standard format for representation of characters in computers.
Select correct option:
True
False

MUL (multiply) Instruction performs an unsigned multiplication of the source operand and the _____.
Select correct option:
Accumulator
Carry

Word
Base

We can convert any digit to __ by adding 0x30 in the digit. Select correct option:
Character
ASCII
EBCDIC
Standard Code

A typical stack is an area of computer memory with a fixed origin and a variable

True

False

Local variables should be created when the subroutine is called and discarded afterwards.

True

False

Both DS and ES can be used to access the video memory. However we commonly keep DS for accessing our data, and load ES with the segment of video memory.

True

False

Elements are removed from the stack in the reverse order to the order of their addition.

True

False

The Operation of Push is if "we push ax" then SP<-- SP+2 [SP]<-- AX

True

False

The operations of placing items on the stack and removing them from there are called push and ret.

True

False

A _____ is an area of memory that holds all local variables and parameters used by any function and remembers the order in which functions are called so that function returns occur correctly.

Instruction Pointer

Stack

Data Segment

Base Register

Stack is a data structure that behaves in a first in last _____ manner.

In

Out

Push

Add

RET do not pops the word at the top of the stack (pointed to by register SP) into the instruction pointer but increments SP by two.

True

False

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