Virtual University	CS302-Degital Logic Design (Solved Macq's) LECTURE FROM (23 to 45)	VU LMS HELP vulmshelp.com
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Question No: 1
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
► Set-up time
► **Hold time (Page 242)**
► Pulse Interval time
► Pulse Stability time (PST)

Question No: 2
74HC163 has two enable input pins which are_____and _____
► **ENP, ENT (Page 285)**
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 3
_____is said to occur when multiple internal variables change due to change in one input variable
► Clock Skew
► **Race condition (Page 267)**
► Hold delay
► Hold and Wait

Question No: 4
The_____input overrides the_____input
► **Asynchronous, synchronous (Page 369)**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 5
A decade counter is_____.
► Mod-3 counter
► Mod-5 counter
► Mod-8 counter
► **Mod-10 counter (Page 274)**

Question No: 6
In asynchronous transmission when the transmission line is idle, _____
► It is set to logic low
► **It is set to logic high (Page 356)**
► Remains in previous state
► State of transmission line is not used to start transmission

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Question No: 7 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8",_____clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356)**

Question No: 8

In a sequential circuit the next state is determined by_____and _____

► State variable, current state
► Current state, flip-flop output
► **Current state and external input (Page 318)**
► Input and clock signal applied

Question No: 9

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Question No: 10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► **True (Page 221)**
► False

Question No: 11

A Nibble consists of_____bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 12

Excess-8 code assigns_____to "-8"

► 1110
► 1100
► 1000
► **0000 (Page 34)**

Question No: 13

The voltage gain of the Inverting Amplifier is given by the relation _____

► **Vout / Vin = - Rf / Ri (Page 446)**
► Vout / Rf = - Vin / Ri
► Rf / Vin = - Ri / Vout
► Rf / Vin = Ri / Vout

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Question No: 14
LUT is acronym for _____
► **Look Up Table (Page 439)**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 15
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

Question No: 16
The total amount of memory that is supported by any digital system depends upon _____
► The organization of memory
► The structure of memory
► The size of decoding unit
► **The size of the address bus of the microprocessor (Page 430)**

Question No: 17
Stack is an acronym for _____
► FIFO memory
► **LIFO memory (Page 429)**
► Flash Memory
► Bust Flash Memory

Question No: 18
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► **127**
► 345

Question No: 19
_____is one of the examples of synchronous inputs.
► **J-K input (Page 235)**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 20
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
► Race condition
► **Clock Skew (Page 226)**

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► Ripple Effect
► None of given options

Question No: 22
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 23
_____is used to simplify the circuit that determines the next state.
► State diagram
► Next state table
► State reduction
► **State assignment (Page 335)**

Question No: 24
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. Wha will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
► 1100
► 0011
► 0000
► 1111

Question No: 25
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 26
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356)**
► Serial data to serial
► Parallel data to parallel

Question No: 27
GAL is essentially a_____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

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Question No: 28
in_____, all the columns in the same row are either read or written.
► Sequential Access
► MOS Access
► **FAST Mode Page Access (Page 413)**
► None of given options

Question No: 29
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 30
A flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 31
A frequency counter _____
► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301)**
► Counts high and low range of given clock pulse
► None of given options

Question No: 32
In a sequential circuit the next state is determined by_____and _____
► State variable, current state
► Current state, flip-flop output
► Current state and external input
► **Input and clock signal applied (Page 305)**

Question No: 33
Flip flops are also called _____
► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

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Question No: 36

Given the state diagram of an up/down counter, we can find _____

► **The next state of a given present state (Page 371)**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

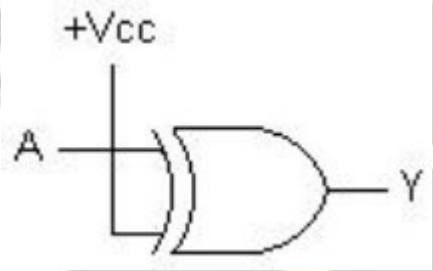
Question No: 38

A Nibble consists of_____bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 39

The output of this circuit is always_____.



► 1
► 0
► A
► $\overline{A}$

Question No: 40

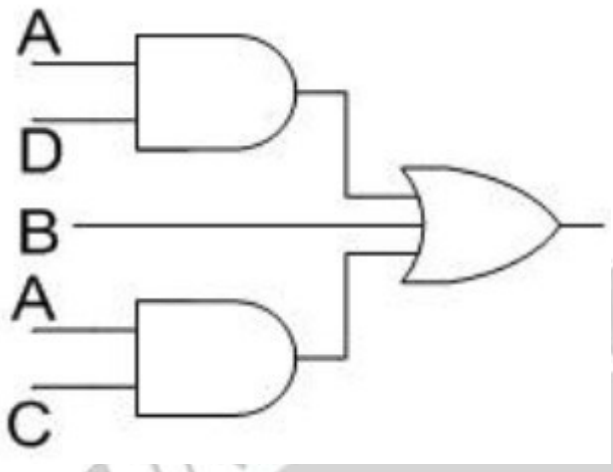
A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of_____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► **two AND gates, one OR gate, two inverters (Lecture 8)**
► two AND gates, one OR gate

Question No: 41

The diagram given below represents _____

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► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

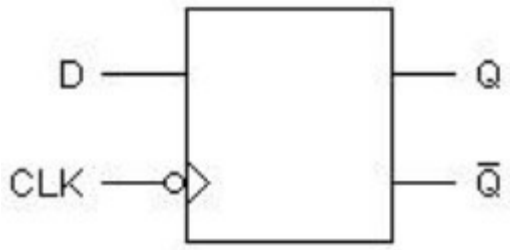
Question No: 42
The voltage gain of the Inverting Amplifier is given by the relation _____
► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 43
DRAM stands for _____
► **Dynamic RAM (Page 407)**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 44
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page**

40) Question No: 45

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Which of the following statement is true regarding above block diagram?
► Triggering takes place on the negative-going edge of the CLK pulse
► Triggering takes place on the positive-going edge of the CLK pulse
► Triggering can take place anytime during the HIGH level of the CLK waveform
► Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 46
The expression F=A+B+C describes the operation of three bits_____Gate.
► **OR (Page 42)**
► AND
► NOT
► NAND

Question No: 47
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► **127**
► 345

Question No: 48
The ANSI/IEEE Standard 754 defines a_____Single-Precision Floating Point format for binary numbers.
► 8-bit
► 16-bit
► **32-bit (Page 25)**
► 64-bit

Question No: 49
The decimal "17" in BCD will be represented as _____
► 11101
► 11011
► **10111 (According to rule)**
► 11110

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Question No: 50
The basic building block for a logical circuit is _____
► A Flip-Flop
► **A Logical Gate (Page 7)**
► An Adder
► None of given options

Question No: 51
The output of the expression F=A.B.C will be Logic_____when A=1, B=0, C=1.
► Undefined
► One
► **Zero (According to rule)**
► No Output as input is invalid.

Question No: 52
_____is invalid number of cells in a single group formed by the adjacent cells in K-map
► 2
► 8
► **12 (According to rule "2^n")**
► 16

Question No: 53
The PROM consists of a fixed non-programmable_____Gate array configured as a decoder.
► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 54
_____is one of the examples of asynchronous inputs. ► J-K input
► S-R input
► D input

► **Clear Input (CLR) (Page 235)** **Question No: 55**
Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____
► 0000
► **1101 (not sure)**
► 1011
► 1111

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Question No: 56

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 57

_____is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

Question No: 59

The best state assignment tends to_____.

► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
► Minimizes the number of state variables that don't change in a group of related states
► Minimize the equivalent states
► None of given options

Question No: 60

5-bit Johnson counter sequences through_____states

► 7
► **10 (Page 354)**
► 32
► 25

Question No: 61

The address from which the data is read, is provided by _____

► Depends on circuitry
► None of given options
► RAM
► **Microprocessor (Page 397)**

Question No: 62

FIFO is an acronym for _____

► **First In, First Out (Page 424)**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 63

The voltage gain of the Inverting Amplifier is given by the relation _____

► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**

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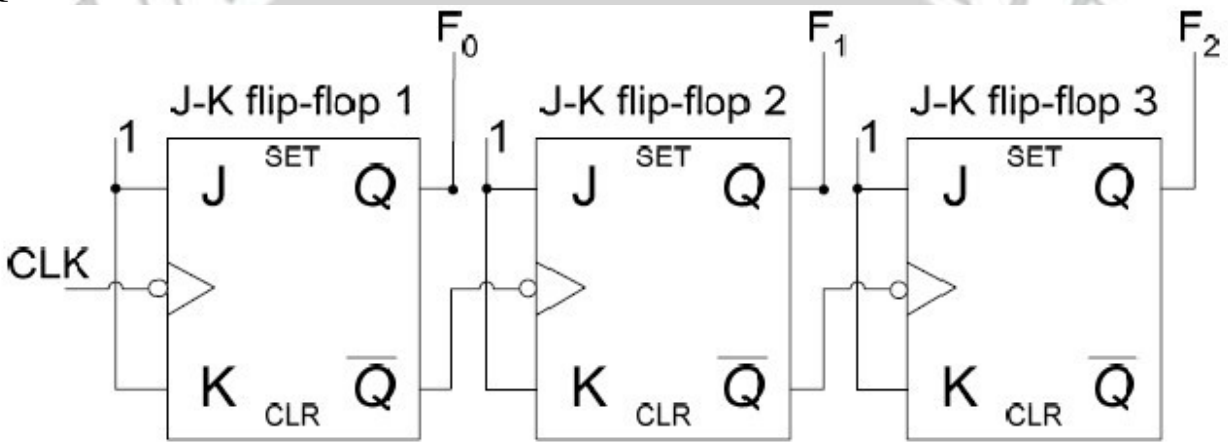
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 64

_____of a D/A converter is determined by comparing the actual output of a D/A converter with the expecte output.

► Resolution
► **Accuracy (Page 460)**
► Quantization
► Missing Code

Question No: 65



Above is the circuit diagram of_____.

► **Asynchronous up-counter (Page 270)**
► Asynchronous down-counter
► Synchronous up-counter
► Synchronous down-counter

Question No: 66

The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354)**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

Question No: 67

"A + B = B + A" is _____

► Demorgan"s Law
► Distributive Law
► **Commutative Law (Page 72)**
► Associative Law

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Question No: 68

Following is standard POS expression

$$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$$

► **True (Lecture 9)**
► False

Question No: 69

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

► Using a single comparator
► **Using Iterative Circuit based Comparators (Page 155)**
► Connecting comparators in vertical hierarchy
► Extra logic gates are always required.

Question No: 70

DE multiplexer is also called

► Data selector
► Data router
► **Data distributor (Page 178)**
► Data encoder

Question No: 71

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 72

_____Counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**
► Synchronous
► Positive-Edge triggered
► Negative-Edge triggered

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Question No: 74
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 75
A synchronous decade counter will have_____flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 76
The alternate solution for a demultiplexer-register combination circuit is _____
► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 77
The 4-bit 2"s complement representation of "+5" is _____
► 1010
► 1110
► 1011
► **0101 (Page 22)**

Question No: 78
The storage cell in SRAM is
► a flip –flop
► **a capacitor (Page 407)**
► a fuse
► a magnetic domain

Question No: 79
What is the difference between a D latch and a D flip-flop?
► The D latch has a clock input.
► The D flip-flop has an enable input.
► The D latch is used for faster operation.
► **The D flip-flop has a clock input.**

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Question No: 80

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs Will _____ if the clock goes HIGH.

► **toggle**
► set
► reset
► not change

Question No: 81

The OR gate performs Boolean_____.

► multiplication
► subtraction
► division
► **addition (Page 42)**

Question No: 82

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

► **set (Page 219)**
► reset
► invalid
► clear

Question No: 83

Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.

► A = 1, B = 0, C = 0, D = 0
► **A = 1, B = 0, C = 1, D = 0 (Lecture 8)**
► A = 0, B = 1, C = 0, D = 0
► A = 1, B = 0, C = 1, D = 1

Question No: 84

The power dissipation, *P*D, of a logic gate is the product of the

► **dc supply voltage and the peak current**
► dc supply voltage and the average supply current
► ac supply voltage and the peak current
► ac supply voltage and the average supply current

Question No: 85

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True**
► False

Question No:86

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **True (Page 50)**
► False

Question No: 87

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Using multiplexer as parallel to serial converter requires_____connected to the multiplexer

► A parallel to serial converter circuit (Page 244)

► A counter circuit

► A BCD to Decimal decoder

► A 2-to-8 bit decoder

Question No: 88

The 3-variable Karnaugh Map (K-Map) has_____cells for min or max terms

►4

► 8 (Page 89)

► 12

► 16

Question No: 89

In designing any counter the transition from a current state to the next sate is determined by

► Current state and inputs (Page 332)

► Only inputs

► Only current state

► current state and outputs

Question No: 90

Sum term (Max term) is implemented using_____gates

► OR (Page 78)

► AND

► NOT

► OR-AND

Question No: 91

AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

►2

►4

►6

► 8 (not sure)

Question No: 93

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

►0

► 1 (Page 230)

► Invalid

► Input is invalid

Question No: 94

If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop

► 0

► 1

► Invalid (Page 233)

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► Input is invalid

Question No: 95

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help h

_____

►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 96

A counter is implemented using three (3) flip-flops, possibly it will have_____maximum output status.

►3
►7
►8 (Page 272)
►15

Question No: 97

In_____Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 98

The_____of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 99

Bi-stable devices remain in either of their_____states unless the inputs force the device to switch its state

►Ten
►Eight
►Three
►Two (Page 262)

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Question No: 101

A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

►= 0, Cout = 0

►= 0, Cout = 1 (Page 135)

►= 1, Cout = 0

►= 1, Cout = 1

Question No: 102

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

► GATED FLIP-FLOPS

► PULSE TRIGGERED FLIP-FLOPS

► POSITIVE-EDGE TRIGGERED FLIP-FLOPS

► NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)

Question No: 103

The design and implementation of synchronous counters start from _____

► Truth table

► k-map

► state table

► state diagram (Page 319)

Question No: 104

THE HOURS COUNTER IS IMPLEMENTED USING _____

► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED

► MOD-10 AND MOD-6 COUNTERS

► MOD-10 AND MOD-2 COUNTERS

► A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)

Question No: 105 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

► 1 floating-gate MOS transistor (Page 419)

► 2 floating-gate MOS transistors

► 4 floating-gate MOS transistors

► 6 floating-gate MOS transistors

Question No: 106 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

► Q2:= Q1 $ X $ Q3

► Q2:= Q1 # X # Q3 (Page 210)

► Q2:= Q1 & X & Q3

► Q2:= Q1 ! X ! Q3

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Question No: 107

Generally, the Power dissipation of_____devices remains constant throughout their operation.

► TTL (Page 65)

► CMOS 3.5 series

► CMOS 5 Series

► Power dissipation of all circuits increases with time.

Question No: 108

When the control line in tri-state buffer is high the buffer operates like a_____gate

► AND

► OR

► NOT (Page 196)

► XOR

Question No: 109

3.3 v CMOS series is characterized by_____and_____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation

► Fast switching speeds, high power dissipation

► Fast switching speeds, very low power dissipation (Page 61)

► Low switching speeds, very low power dissipation

Question No:110

The output of an AND gate is one when _____

► All of the inputs are one (Page 40)

► Any of the input is one

► Any of the input is zero

► All the inputs are zero

Question No: 111

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1

► A > B = 0, A < B = 1, A = B = 0

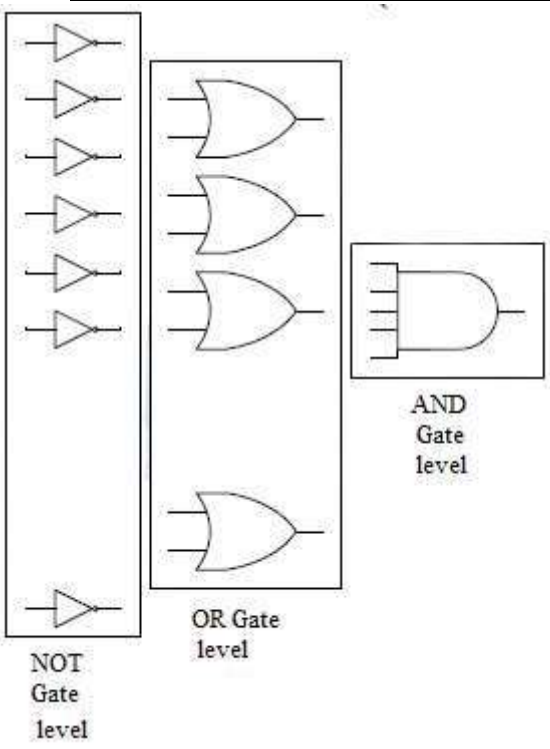
► A > B = 1, A < B = 0, A = B = 0 (Page 109)

► A > B = 0, A < B = 1, A = B = 1

Question No:112

The diagram above shows the general implementation of_____form

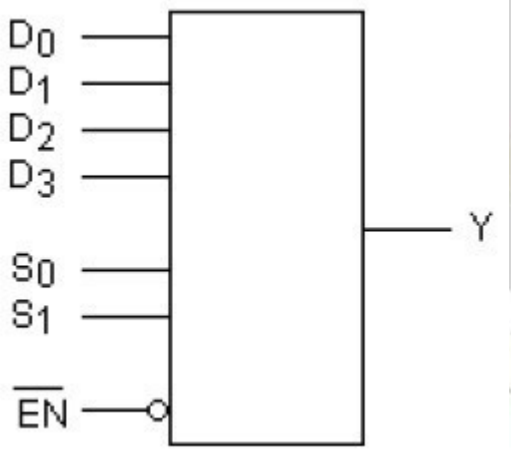
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- ► boolean
- ► arbitrary
- ► **POS (Page 122)**
- ► SOP

Question No: 113

The device shown here is most likely a



- ► Comparator
- ► Multiplexer
- ► Demultiplexer
- ► Parity generator

Question No: 114

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DE multiplexer converts_____data to_____
data
► Parallel data, serial data
► **Serial data, parallel data (Page 356)**
► Encoded data, decoded data
► All of the given options.

Question No:115
If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop
► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 116
If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop
► 0
► 1
► **Invalid (Page 230)**
► Input is invalid

Question No: 119
In asynchronous digital systems all the circuits change their state with respect to a common clock
► True
► **False (Page 245)**

Question No: 201
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 202
A divide-by-50 counter divides the input_____signal to a 1 Hz signal.
► 10 Hz
► **50 Hz (Page 298)**
► 100 Hz
► 500 Hz

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Question No: 203
The design and implementation of synchronous counters start from _____
► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 204
In_____the output of the last flip-flop of the shift register is connected to the data input of the first flip-flop. ► Moore machine
► Mealy machine
► **Johnson counter (Page 354)**
► Ring counter Q

Question No: 205
Which is not characteristic of a shift register?
► **Serial in/parallel in (Page 346)**
► Serial in/parallel out
► Parallel in/serial out
► Parallel in/parallel out

Question No:206
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
► FALSE
► **TRUE (Page 250)**

Question No: 207
The output of an XNOR gate is 1 when_____I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one
► I Only
► IV Only
► I and IV only
► **II and III only (Page 53)**

Question No: 208
NAND gate is formed by connecting _____
► **AND Gate and then NOT Gate (Page 45)**
► NOT Gate and then AND Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

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Question No: 209

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

► Zero

► **One (Page 46)**

► Undefined

► No output as input is invalid

Question No: 210

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

► Radiation-Erase programming method (REPM)

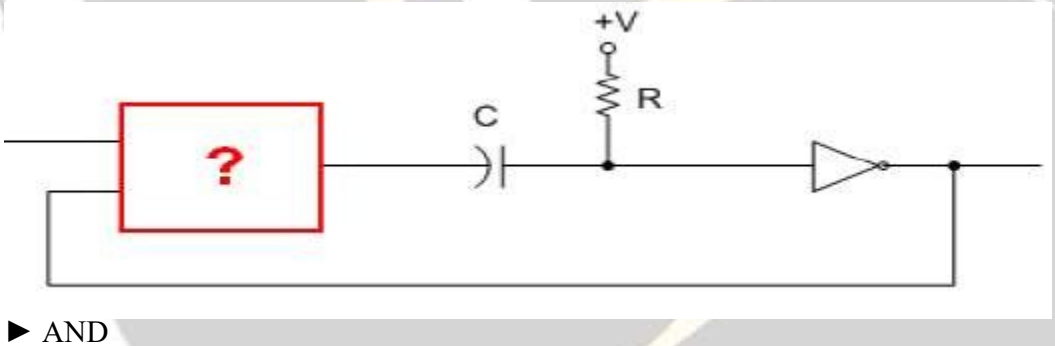
► **In-System Programming (ISP) (Page 194)**

► In-chip Programming (ICP)

► Electronically-Erase programming method(EEPM)

Question No: 211

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



► AND

► NAND

► NOR

► **XNOR (Page 262)**

Question No: 212

In_____outputs depend only on the combination of current state and inputs.

► **Mealy machine (Page 332)**

► Moore Machine

► State Reduction table

► State Assignment table

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Question No: 213
In the following statement Z PIN 20 ISTYPE „reg.invert“;
The keyword “reg.invert” indicates _____
► An inverted register input
► An inverted register input at pin 20
► Active-high Registered Mode output
► **Active-low Registered Mode output (Page 360)**

Question No: 214
A Nibble consists of_____bits
► 2
► **4 (Page 394)**
► 8
► 16

Question No: 215
A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to b
entered on the serial data-input line. After two clock pulses, the shift register is storing_____.
► 1110
► 0111
► 1000
► **1001**

Question No: 216
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 217
If the FIFO Memory output is already filled with data then _____
► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 218
The process of converting the analogue signal into a digital representation (code) is known as _____
► Strobing
► Amplification
► **Quantization (Page 445)**
► Digitization

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Question No: 219

$(A + B)(A + \overline{B} + C)(\overline{A} + C)$

is an example of _____

► **Product of sum form (Page 77)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 220

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

► Q2:= Q1 $ X $ Q3
► **Q2:= Q1 # X # Q3 (Page 210)**
► Q2:= Q1 & X & Q3
► Q2:= Q1 ! X ! Q3

Question No: 221

Caveman number system is Base_____number system ► 2

► **5 (Page 11)**
► 10
► 16

Question No: 222

The output of an XOR gate is zero (0) when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 223

The simplest and most commonly used Decoders are the_____Decoders

► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

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Question No: 224
The_____Encoder is used as a keypad encoder.
► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 225
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
► **True (Page 161)**
► False

Question No: 226
If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop
► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 227
If the S and R inputs of the gated S-R latch are connected together using a_____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)
► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 228
The low to high or high to low transition of the clock is considered to be a(n) _____
► State
► **Edge (Page 228)**
► Trigger
► One-shot

Question No: 230
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 231
A transparent mode means _____
► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

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Question No: 232
In_____outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 233
Smallest unit of binary data is a _____
► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 234
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 235
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 236
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT_____GATE
► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 237
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.
► **TRUE (Page 182)**
► FALSE

Question No: 241
A synchronous decade counter will have_____flip-flops
► 3
► **4 (Page 281)**
► 7

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► 10

Question No: 242

The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356)**

► Serial in / Parallel out shift register

► Parallel in / Parallel out shift register

► Serial in / Serial Out shift register

Question No: 243

A 8-bit serial in / parallel out shift register contains the value "8",_____clock signal(s) will be required to shift the value completely out of the register.

► 1

► 2

► 4

► **8 (Page 356)**

Question No: 245

If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter

► It is not locked; the new data overwrites the previous data.

► Previous data is swapped out of memory and new data enters

► **None of given options**

Question No: 246

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO ------

► THE FLOP-FLOP IS TRIGGERED

► Q=0 AND Q‟=1

► Q=1 AND Q‟=0

► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)** **Question No: 247**

The terminal count of a 4-bit binary counter in the UP mode is____.

- 1100
- 0011
- 1111
- 0000

Question No: 248

For a down counter that counts from (111 to 000). If current state is "101" the next state willbe ____.

- 111
- 110
- 010
- None of given options

Question No: 249

The n flip-flops store_____states.

a. 1

b.

2^n

c. 0

d. 2^(n+1)

Question No: 250

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting _____.

- Q output of all flip-flops to clock input of next flip-flops
- Q' output of all flip-flops to clock input of next flip-flops
- Q output of all flip-flops to J input of next flip-flops
- Q' output of all flip-flops to K input of next flip-flops

Question No: 251

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together.

- True
- False

Question No: 251

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

a.True

b.False

Question No: 252

The 74HC163 is a 4-bit Synchronous Counter, it has_____data output pins.

b. 2

b. 4

c. 6

d. 8

Question No: 253

Divide-by-32 counter can be achieved by using

c. Flip-Flop and DIV10b. Flip-Flop and DIV 16

c. Flip-Flop and DIV 32

d. DIV 16 and DIV 32

Question No: 254

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The synchronous counters are also known as Ripple Counters:

a.True

b False

Question No: 255

Each stage of Master-slave flip-flop works at_____of the clock signal

- Each stage works on complete clock signal
- One fourth
- One third
- One half

Question No: 256

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

`

a. 80 micro seconds

b. 8 micro seconds

c. 80 mili seconds

d. 10 micro seconds

Question No: 257

Number of states in an 8-bit Johnson counter sequence are:

d. 8

e. 12

f. 14

g. 16

Question No: 258

In moore machine the output depends on

- The current state and the output of previous flip flop
- Only inputs
- The current state
- The current state and inputs

Question No: 259

Asynchronous mean that _____

- Each flip-flop after the first one is enabled by the output of the preceding flip-flop
- Each flip-flop is enabled by the output of the preceding flip-flop
- Each flip-flop except the last one is enabled by the output of the preceding flip-flop
- Each alternative flip-flop after the first one is enabled by the output of the precedingflip-flop

Question No: 260

According to moore circuit, the output of synchronous sequential circuit depend/s on _____of flip flop.

h. Previous state

i. Present state

j. Next state

k. External state

Question No: 261

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

- Q
- 0
- 1
- Invalid

Question No: 262

A Divide-by-20 counter can be achieved by using

a. Flip-Flop and DIV 10
b. Flip-Flop and DIV 16
c. Flip-Flop and DIV 32
d. DIV 10 and DIV 16

Question No: 263

A one-shot mono-stable device contains_____

- AND gate, Resistor, Capacitor and NOT Gate
- NAND gate, Resistor, Capacitor and NOT Gate
- NOR gate, Resistor, Capacitor and NOT Gate
- XNOR gate, Resistor, Capacitor and NOT Gate

Question No: 264

The_inputs can be directly mapped to karnaugh maps.

- S-R
- J-K
- Flip-Flop
- External

Question No: 265

A mono-stable device only has a single stable state

a. True
b. False

Question No: 266

When the_____Hz sampling interval is selected, the signal at the output of the J-K flip-flophas a time period of_____seconds.

a. 1, 2
b. 0, 2
c. 2, 5
d. 1, 1

Question No: 267

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to_____.

- Set
- Toggle

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- Latch
- Reset

Question No: 268

A stage in the shift register consists of

- A latch
- A flip flop
- A byte of storage
- Four bits of storage

Question No: 269

If a circuit suffers "Clock Skew" problem, the output of circuit can't be guarantied.

a. True
b. False

Question No: 270

A modulus-14 counter has fourteen states requiring _____

l. 14 flip flops
m. 14 registers
c. 4 flip flops
d. 4 registers

Question No: 271

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using_____gate.

- AND
- OR
- NOT
- NAND

Question No: 272

_____flip-flops are obsolete now.

- Edge-triggered
- Master-Slave
- T-flipflop
- D-flipflop

Question No: 273

The glitches due to "Race Condition" can be avoided by using a_____.

n. Gated flip-flops
o. Pulse triggered flip-flops
p. Positive-Edge triggered flip-flops
d. Negative-Edge triggered flip-flops

Question No: 274

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=_____

- 0
- Q(t)

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- 1

- Invalid

Question No: 275

____occurs when the same clock signal arrives at different times at different clockinputs due to propagation delay.

q. Race condition
b. Clock skew
c. Ripple effect
d. None of given options

Question No: 276

An Astable multivibrator is known as a (n)_____.

a. Oscillator
b. Booster
c. One-shot
d. Dual-shot

Question No: 277

In Master-Slave flip-flop setup, the master flip-flop operators at _____

- Positive half cycle of pulse
- Negative half cycle of pulse
- Both Master-Slave operator simultaneously
- Master-Slave flip-flop does not operate on pulses rather it is edge triggered

Question No: 278

The power consumed by a flip-flop is defined by _____

- P = Icc x Rcc
- P=vcc x Rcc
- c.P = Vcc x Icc
- P = Mcc x Vcc

Question No: 279

The 3-bit up counter can be implemented using_____flip-flop(s).

- S-R flip-flops only
- S-R flip-flops and D-flip-flops
- S-R flip-flops or D-flip-flops
- D-flip-flop only

Question No: 280

The terminal count of a 4-bit binary counter in the DOWN mode is _____

a. 0000
b. 0011
c. 1100
d. 1111

Question No: 281

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

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- State reduction
- State minimization

State assignment

- State evaluation

Question No: 282

State of flip-flop can be switched by changing its _____

a. Input signal
b. Output signal
c. Momentary signal
d. Contemporary signal

Question No: 283

Once the state diagram is drawn for any sequential circuit the next step is to draw

- Transiation table
- Karnaugh map
- Next-state table
- Logic expression

Question No: 284

Design of state diagram is one of many steps used to design

- A clock
- A truncated counter
- An UP/DOWN counter
- Any counter

Question No: 285

Flip flops are also called _____

- Bi-stable multivibrators
- Bi-stable singlevibrators
- Bi-stable dualvibrators
- Bi-stable transformer

Question No: 286

Three cascaded modulus-10 counters have an overall modulus of

- 30
- b. 100
- c. 1000

➢ 10000

Question No: 287

The term hold always means_____.

a. Q=0, Q'=1
b. Q=1, Q'=0
c. Q=0, Q'=0
d. No change

Question No: 288

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

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a. J=1, K=0
b. J=1,K=X(Don't care)
c. J=X(Don't care),K=0
d. J=0, K=X(Don't care)

Question No: 289

To parallel load a byte of data into a shift register, there must be

a. One clock pulse
b. One clock pulse for each 1 in the data
c. Eight clock pulse
d. One clock pulse for each 0 in the data

Question No: 290

Invalid state of NOR based SR latch occurs when_____.

r. S=0, R=0
s. S=0, R=1
t. S=1, R=0
u. S=1, R=1

1. The transition table is very similar to the_____table
   a. Truth
   b. State page 382
   c. Transition
   d. None of the given option

2. Two Signals_____and_____provide the timing inputs to the state machine
   a. NSSR and EWSR
   b. LTIME and STIME page 374
   c. PTIME and QTIME
   d. NSGrn and NSYel
3. Memories are implemented in_____bit data unit sizes
   a. 1 , 2 and 6
   b. 2 , 3 and 6
   c. 1 , 4 and 8 page 425
   d. 4 , 5 and 8
4. In distributed mode, for a 1024 X 1024 DRAM memory and a refresh cycle of8msec, each of the 1024 rows has to be refreshed in_____when distributed refresh is used
   a. 4.8 microsec
   b. 5.9 micorsec
   c. 7.8 micorsec page 406

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d. 5.5 microsec

5. The EPROM uses_____array with an isolated gate structurea. NMOSFET page 411
   b. MOSFETK
   c. UVMOSFT
   d. None of the given options
6. The 64-cell array organized as 8 X 8 cell array is considered
   a. As an 64 byte memory
   b. As a 16 byte memory
   c. As an 8 byte memory page 387
   d. As an 4 byte memory
7. The test vector definition defines the test vector for all the three counter inputsand___counter output/outputs
   a. One
   b. Two
   c. Three page 362
   d. Four
8. In memory write cycle, the time for which the WE signal remains active isknown as the _____
   a. Write address setup
   b. Write pulse width page 397
   c. Write delay width
   d. Write Data Time

9. If the voltage drop across the active load is 0 volts due to absence of current thecomparator output is a_____
   a. 0
   b. 1 page 417
10. As data values are written or read from RAM stack, the stack pointer registerincrements or decrements its contents always pointing to the stack

    a. Bottom
    b. Top page 422
    c. Down
    d. Vertex
11. A 4-bit binary up/down counter in in the binary state of zero. The next state inthe DOWN mode is?
    a. 0001
    b. 1000

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c. 1110
d. 1111

12. Flash memory operation are classified into_____different operations
    a. Two
    b. Three page 413
    c. Four
    d. Five
13. Implementation of latch is required almost_____transistor?
    a. Two
    b. Four
    c. Six page 417
    d. Eight
14. In elevator circuit, the floor display circuit is a combinational circuit which usesthe_____and_____inputs two determine the floor number and the function of the display arrow.
    a. CONSTATE, FB
    b. OPEN, DIR
    c. MOTION, DIR page 374
    d. MOTION, FB

15. The bit capacity of memory that has 1024 addresses and can store 8 bit at eachaddress is
    a. 8
    b. 1024
    c. 4096
    d. 8192 page 388(memory capacity) 1024*8=8192
16. When the transmission line is idle in an asynchronous transmission
    a. It is set to logic low
    b. It set to logic high page 349
    c. It remains in previous state
    d. State of transmission line is not used to start transmission17.Which of the following is a volatile memory?
    a. PROM
    b. DRAM page 400(capacitor based ROM, need extra circuit to retain the memory)
    c. EPROM
    d. EEPROM
18. Which signal must remain valid in memory write cycle after data is applied atthe data input lines and must remain valid for a minimum time duration t_{WD} ?

a. `CS
b. `WE page 397
c. W
d. OE

19. The ROM used by computer is relatively very_____as it stores fewbytes of code used to boot the computer system on power up
a. Small page 423
b. Large
c. Heavy
d. High

20. In DRAM read cycle R/W signal is activated to read data which is madeavailable on the_____Data line
a. D(IN)
b. D(OUT) page 405
c. D(AB)
d. D(INT)

21. _____Yellow signal controlling the traffic on the east–westsection.
a. NSGrn
b. NSYel
c. EWYel page 375
d. EWRed

22. A 32 bit data word consists of :
a. 2 bytes
b. 4 Bytes page 387
c. 2 nibbles
d. 4 nibbles

23. A complete unit of information is sometimes called a _____
a. Bit
b. Nibble
c. Word(correct) page 387
d. Byte

24. Memory is arranged in
a. Liner fashion
b. Two dimensional manner page 396
c. Three dimensional manner
d. Random fashion

25. Which of the following output equations determines the output of the

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statemachine?

a. MIN = Q0Q1
b. MAX = Q0Q1EN page 382
c. MIN = Q0Q1EN
d. MAX = Q1EN

26. A multiplexer with the register circuit convert
    a. Serial data to parallel
    b. Parallel data to serial page 349
    c. Serial data to serial
    d. Parallel data to parallel
27. The chip enable access time which is the timer for the validated data to appearafter the_____transition of the chip select signal CS
    a. high to high
    b. high to low page 397
    c. low to high
    d. low to low
28. The duration for which the elevator doors are opened , and remain open,, and time it takes for elevator to move from one floor to the next can be determinedby a/an__
    a. input signal
    b. output signal
    c. clock signal page 365
    d. None of Given
29. The ABEL input file can use a_____instead of the equation to specify theBoolean expression
    a. truth table page 370
    b. state diagram
    c. karnaugh map
    d. logical circuit
30. Implementation of the FIFO buffer in RAM is usually takes the form of a _____buffer
    a. Circular page 420
    b. Rectangular
    c. Triangular
    d. Square
31. How many state variables does each state in Traffic Light Controller have?
    a. One
    b. Two

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c. Three page 377

d. Four

32. The output of SR latches in elevator state machine are generated bycombinational circuit therefore these output are defined as

ISTYPE_____

a. Com.reg

c. Com.buffer page 372

b. Com.org

d. Reg.buffer

33. When an eight bit serial in/out shift register is used for 24 micro second timedelay the clock frequency must be

a. 41.67 KHz

b. 333 KHs

c. 125 KHs

d. 8 MHz

34. Which of the following memories uses one transistor and one capacitor as basicmemory unit?

a. SRAM

b. DRAM page 400

c. PRAM

d. TRAM

35. A divide by 10 ring counter requires a minimum ofa. Ten flip flops

b. Five flip flops

c. Four flip flops

d. Twelve filp flops

35. Which one flip flop has an invalid output state?

a. T

b. J

Kc.

SR

d. D

36. In the keyboard encounter how many times per second does the ring counter santhe keyboard

a. 600scans./seco

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nb. 625 scan/second
c. 650 scan/second
d. 700 scan/second

37. Smallest unit of data isa. a bit
b. a 4 bit nibbles
c. an 8 bit word
d. a 16 bit word

38. The output of SR latches in elevator state machine are feed back to the _____gate array for connection of D Flip Flops
a. NO
Tb. AND
c. OR
d. XOR

39. The static RAM(SRAM) is non-volatile and is not a_____density memory aslatch is required to store a single bit of information
a. Lo
wb. High
c. Medium
d. Hot

40. Choose the best possible answer of the following question.
The D flip flop is only activated by _____
a. A negative edged triggerb. A positive edged trigger
c. Both positive and negative edge triggered
d. None of the given options

41. The Fast mode page access allows_____memory read and access time when reading successive data values stored in connective locations on the samerow
a. Slo
w b. Faster
c. Medium
d. Modern

42. The next state table for REQ1, FLOOR1 and OPEN input indicates that the

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_____can be pressed at any time either on the first floor or the second floor inelevator

a. REQ0
b. Open
c. REQ I
d. FLOOR1

49.A 4-bit binary up/down counter in in the binary state of zero. The next state in the UP mode is?

- 0001
- 1000
- 1110
- 1111

50. In memory read cycle, the read cycle is initiated by
    a. Providing data to the variable
    b. Applying data to signals
    c. Applying the address signals
    d. Providing arithmetic operations
51. FLASH memory cell is implemented using a single floating gate _____ transistor
    a. MOS
    b. LOS
    c. GOS
    d. POS
52. UVEPROM is stands for
    a. Ultra Variant
    b. Ultra Vibrant
    c. Ultra Violet
    d. Ultra Visible
53. Four 4k byte chips can be connected together to implement wordmemory
    a. 10K
    b. 15K
    c. 16 K
    d. 8K
54. There are_____basic type of EPROM

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a. Two
b. Three
c. Four
d. Five

55. Two type of memories namely the first in first out(FIFO) memory and last infirst out (LIFO) are implemented using _____
    a. Shift Register
    b. Circular Buffer
    c. Ring Buffer
    d. Reduce Registers

56. A memory organized to store nibble data values requires a _____wide databus
    - 2 bit
    - 4 bit
        - 8 bit
    - 16 bit

57. ROMs and PROMs retains information_____even if the supply voltage isremoved.
    a. For one day
    b. For seven days
    c. For ten days
    d. Permanently

58. You have to choose suitable option when your timer will reset by consideringthis given code:

```
TRSTATE.CLK = clk:
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
```

    a. NSY2 or EWY2
    b. NSSR or TMRST
    c. EWSR or NSRED
    d. EWRed or EWYel

59. Synchronous SRAM uses a clock signal which is used by the tosynchronize its activities.
    a. ALU
    b. Control Unit
    c. Microprocessor
    d. Address Bus

60. Implementation of the FIFO buffer in_____is usually takes the form

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of acircular buffer

a. RAM page 420
b. ROM
c. PROM
d. Flash Memory

The CONSTATE.CLK = Clock is used to indicate that the___statevariables change on a clock

57. The CONSTATE.CLK = Clock is used to indicate that the statevariables change on a clock transition.
    a. CONSTATE
    b. FLOOR
    c. MOTION
    d. OPEN

58. The normal data inputs to a flip flop (D,S and R,J and K,T are referred) to as _____inputs
    a. Sequential
    b. Asynchrono us
    c. Synchronous
    d. Combinational

59. The synchronous SRAM also has a burst feature which allows the synchronousSRAM to read or write uptolocation(s) using a single address
    a. One
    b. Two
    c. Three
    d. Four page 399

60. Two State variable allow maximum of_____states
    a. Two
    b. Four page 381
    c. Eight
    d. Sixteen

61. Which of the following is the drawback of DRAM?
    a. Discharging of the capacitor over a period of time
    b. All the information stored in terms if binary bits would be lost ifcapacitor is not recharged

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c. Extra circuit is required to reference the capacitor

d. All of the above are true page 400

62. To write data to the memory the write cycle is initiated by

a. Applying the address signals 397

b. Assigning the values of variable

c. Reserving the space of variables

d. Applying the data signals

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