Sample Paper
FINALTERM EXAMINATION
Fall 2022
CS302 – Digital Logic Design

Time: 90 min
Marks: 60

Question No: 1 (Marks: 01) - Please choose the correct option

Rise and fall in temperature during 24 hours is an example of a?

A. Continuous Quantity
B. Digital Quantity
C. Discrete Quantity
D. Digital & Discrete both

Question No: 2 (Marks: 01) - Please choose the correct option

The Sum-of-Weights method can be used to convert a Binary number of any magnitude to its equivalent.

A. Hexadecimal representation
B. Octal representation
C. Decimal representation
D. Binary representation

Question No: 3 (Marks: 01) - Please choose the correct option

In Binary to Hexadecimal Conversion, the Binary string is divided into small groups of _____ starting from the least significant bit.

A. 1-bits
B. 2-bits
C. 3-bits
D. 4-bits

Question No: 4 (Marks: 01) - Please choose the correct option

F in Hexadecimal is equivalent to _____ in binary.

A. 1111
B. 1011
C. 0011
D. 0000

Question No: 5 (Marks: 01) - Please choose the correct option

The Boolean expression of AND gate is _____

A. Y = A.B
B. Y = A+B
C. Y = A-B
D. Y = A/B

Question No: 6 (Marks: 01) - Please choose the correct option

The logic NOR function is the combination of two logic functions that are _____logics.

A. OR & NOT
B. AND & NOT
C. OR & AND
D. NOT & XOR

Question No: 7 (Marks: 01) - Please choose the correct option

The output of a NAND is _____ when all inputs to the NAND gate are 1s.

A. 1
B. 00
C. 10
D. 0

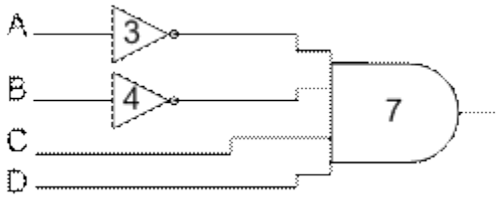
Question No: 8 (Marks: 01) - Please choose the correct option

Demorgan's **First Theorem** states that the complement of a _____ of variables is equal to the sum of the complements of the variables.

A. Sum
B. Subtraction
C. Product page#74

D. Division

Question No: 9 (Marks: 01) - Please choose the correct option



The simplified Boolean expression of this logic circuit is:

A. F = A.B.C.D
B. F = A+B+C+D
C. F = $\bar{A}.\bar{B}.C.D$
D. F = A.B.C+D

Question No: 10 (Marks: 01) - Please choose the correct option

A 4-variable K-Map has an array of _____ cells

A. 8
B. 16
C. 24
D. 32

Question No: 11 (Marks: 01) - Please choose the correct option

A K-map for _____ variables can be constructed by using two 4-variable K-maps.

A. 5
B. 8
C. 15
D. 30

Question No: 12 (Marks: 01) - Please choose the correct option

A standard way to express a Boolean expression is the _____ form.

A. POS
B. SOS
C. POP
D. SOP page# 121

Question No: 13 (Marks: 01) - Please choose the correct option

XOR and _____ gates are used to implement the Odd-Parity Generator Circuit

A. OR
B. XNOR page#133
C. NOR
D. NAND

Question No: 14 (Marks: 01) - Please choose the correct option

The 2's complement of any number is obtained by taking the 1's complement of a number and then _____ a 1 to the 1's complement.

A. Adding
B. Subtracting
C. Multiplying
D. Dividing

Question No: 15 (Marks: 01) - Please choose the correct option

The basic function of a Comparator is to _____ two binary quantities.

A. Multiply & Divide
B. Compare page#153
C. Subtract
D. Add

Question No: 16 (Marks: 01) - Please choose the correct option

The Decimal-to-BCD Encoder has _____ inputs, for the decimal digits 0 to 9 and four outputs corresponding to the 4-bit BCD output.

A. Two
B. Eight
C. Ten page#166
D. Sixteen

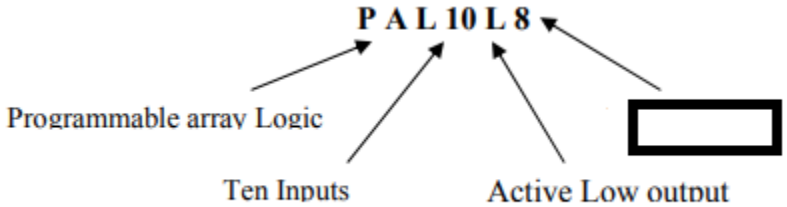
Question No: 17 (Marks: 01) - Please choose the correct option

Demultiplexer has a single input and _____ outputs.

A. Two
B. Three
C. Four

D. Several page#178

Question No: 18 (Marks: 01) - Please choose the correct option



In this figure of Standard PAL Numbering, 8 at the last indicates

A. Eight Inputs
B. Eight Outputs page#187
C. Eight bits
D. Eight Decimals

Question No: 19 (Marks: 01) - Please choose the correct option

ABEL Symbol for Logic operation OR is

A. ! NOT
B. &
C. #
D. $

Question No: 20 (Marks: 01) - Please choose the correct option

A.B in boolean notation is equivalent to _____ in ABEL notation.

A. !A
B. A&B
C. A#B
D. A$B

Question No: 21 (Marks: 01) - Please choose the correct option

Why latches are called memory devices?

A. It can store 8 bits of data
B. It has an internal memory of 4 bit
C. It can store one bit of data
D. It can store an infinite amount of data

Question No: 22 (Marks: 01) - Please choose the correct option

Does the NAND latch work when both inputs are _____?

A. 1
B. 0
C. Inverted
D. Don't care

Question No: 23 (Marks: 01) - Please choose the correct option

The truth table for an S-R flip-flop has how many VALID entries?

A. 1
B. 2
C. 3
D. 4

Question No: 24 (Marks: 01) - Please choose the correct option

Does the basic latch consist of _____?

A. Two inverters
B. Two comparators
C. Two amplifiers
D. Two adders

Question No: 25 (Marks: 01) - Please choose the correct option

In D flip-flop, D stands for _____?

A. Distant
B. Data
C. Desired
D. Delay

Question No: 26 (Marks: 01) - Please choose the correct option

How many stable states do combinational circuits have?

A. 3
B. 4
C. 5
D. 2

Question No: 27 (Marks: 01) - Please choose the correct option

In the serial shifting method, data shifting occurs _____?

A. One bit at a time
B. Two-bit at a time
C. Four bit at a time
D. simultaneously

Question No: 28 (Marks: 01) - Please choose the correct option

The full form of SIPO is _____?

A. Serial-in Parallel-out
B. Parallel-in Serial-out
C. Serial-in Serial-out
D. Serial-In Peripheral-Out

Question No: 29 (Marks: 01) - Please choose the correct option

The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11110000. After two clock pulses, the register contains _____?

A. 10111000
B. 10110111
C. 11110000
D. 11111100

Question No: 30 (Marks: 01) - Please choose the correct option

What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

A. Parallel-in Parallel-out
B. Parallel-in Serial-out
C. Serial-in Serial-out
D. Serial-in Parallel-out

Question No: 31 (Marks: 01) - Please choose the correct option

What is the function of a buffer circuit?

A. To provide an output that is inverted from that of the input
B. To provide an output that is equal to its input

C. To clean up the input
D. To clean up the output

Question No: 32 (Marks: 01) - Please choose the correct option

Which of the following has the lowest access time?

A. RAM
B. ROM
C. Flag
D. Registers

Question No: 33 (Marks: 01) - Please choose the correct option

Logic circuits can also be designed using _____?

A. RAM
B. ROM
C. PLA
D. PLD

Question No: 34 (Marks: 01) - Please choose the correct option

If enable input is high, then the multiplexer is _____?

A. Disable
B. Enable
C. High Impedance
D. Saturation

Question No: 35 (Marks: 01) - Please choose the correct option

A shift register is defined as _____?

A. The register is capable of shifting information either to the right or to the left
B. The register is capable of shifting information to another register
C. The register is capable of shifting information to the left only
D. The register is capable of shifting information to the right only

Question No: 36 (Marks: 01) - Please choose the correct option

Which circuit is generated from D flip-flop due to the addition of an inverter by causing the reduction in the number of inputs?

A. Gated D-latch
B. Gated T-latch
C. Gated JK-latch

D. Gated SR-latch

Question No: 37 (Marks: 01) - Please choose the correct option

When a high is applied to the set line of an SR latch, then_____?

A. Q output goes high
B. Q output goes low
C. Q` output goes high
D. Both Q and Q` go high

Question No: 38 (Marks: 01) - Please choose the correct option

D flip-flop is a circuit having _____?

A. 5 NAND gates
B. 4 NAND gates
C. 3 NAND gates
D. 2 NAND gates

Question No: 39 (Marks: 01) - Please choose the correct option

What is a state diagram?

A. It provides the same information as the state table
B. It is similar to the characteristic equation
C. It provides a graphical representation of states
D. It is the same as the truth table

Question No: 40 (Marks: 01) - Please choose the correct option

How many different states do a 3-bit asynchronous down counter have?

A. 4
B. 6
C. 8
D. 2

Question No: 41 (Marks: 03)

Convert the following hexadecimal number into an equivalent octal number. Also, write down all the steps.

$(A10)_{16}$

Solution:
$(5020)_{8}$

How?

Step 1: Convert each hexadecimal digit to its binary equivalent.

A = 1010 (binary)
1 = 0001 (binary)
0 = 0000 (binary)

Step 2: Combine the binary digits to form a single binary number.

10100001000 (binary)

Step 3: Divide the binary number into groups of 3 bits, starting from the right.

101 000 010 000

Step 4: Convert each group of 3 bits to its octal equivalent.

101 = 5 (octal)
000 = 0 (octal)
010 = 2 (octal)
000 = 0 (octal)

Step 5: Combine the octal digits to form the final octal number.

(5020)8

Therefore, the equivalent octal number for the hexadecimal number (A10)16 is (5020)8.

Note: Hexadecimal to octal conversion involves converting each hexadecimal digit to its binary equivalent, then grouping the binary digits into sets of 3, and finally converting each group to its octal equivalent.

Question No: 42 (Marks: 03)

Convert the following binary number into an equivalent decimal number. Also, write down all the steps.

$(1111111)_2$

Solution:

$(127)_{10}$

How?

Step 1: Write down the binary number with the place values.

2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1	1	1	1	1

Step 2: Multiply each binary digit by its corresponding place value.

1 × 2^6 = 1 × 64 = 64
1 × 2^5 = 1 × 32 = 32
1 × 2^4 = 1 × 16 = 16
1 × 2^3 = 1 × 8 = 8
1 × 2^2 = 1 × 4 = 4
1 × 2^1 = 1 × 2 = 2
1 × 2^0 = 1 × 1 = 1

Step 3: Add up the results of the multiplications.

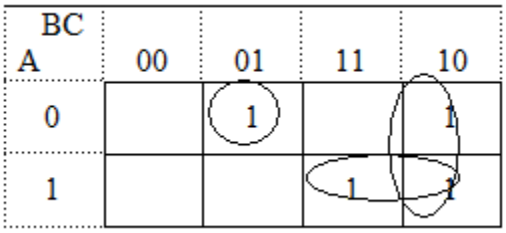
64 + 32 + 16 + 8 + 4 + 2 + 1 = 127

Step 4: Write down the result as the equivalent decimal number.

(1111111)2 = (127)10

Question No: 43 (Marks: 03)

Write the simplified expression for the following table:



Question No: 44 (Marks: 03)

Consider a memory can store 32K nibbles then how many bytes a memory can store? Justify your answer with mathematical proof.

Solution:

=32K nibbles × (1 byte / 2 nibbles) = 32K / 2 bytes

= 16K bytes

Mathematical proof:

Let's denote the number of nibbles as N and the number of bytes as B.

We know that:

1 nibble = 4 bits

1 byte = 8 bits = 2 nibbles

We can write the conversion factor as:

1 nibble = 1/2 byte

Given that the memory can store 32K nibbles, we can set up the equation:

N = 32K nibbles

To find the number of bytes, we can multiply both sides by the conversion factor:

B = N × (1/2 byte/nibble)

= 32K × (1/2)

= 16K bytes

Therefore, the memory can store 16K bytes.

Question No: 45 (Marks: 03)

Apply the shift right operation on the given below 4-bit input and write the output. Consider the 3 clock pulses and write the steps for each pulse.

A = 1011

Solution:

- **Clock Pulse 1:**

- Initial State: A = 1011

- Shift right operation: A = 0101 (rightmost bit 1 is shifted out, and a 0 is filled in the leftmost position)

- Register contents: A = 0101

- **Clock Pulse 2:**

- Current State: A = 0101

- Shift right operation: A = 0010 (rightmost bit 1 is shifted out, and a 0 is filled in the leftmost position)

- Register contents: A = 0010

- **Clock Pulse 3:**

- Current State: A = 0010

- Shift right operation: A = 0001 (rightmost bit 0 is shifted out, and a 0 is filled in the leftmost position)

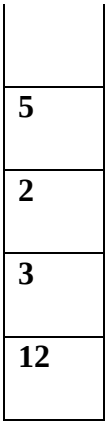
- Register contents: A = 0001

After 3 clock pulses, the output is:

A = 0001

Question No: 46 (Marks: 03)

Consider the state of the stack given below:



Consider the following actions that have been executed and write the final state of the stack.

push 7

pop

pop

SOLUTION

Initial state of the stack (top to bottom) as:

Top -> 5
2
3
Bottom -> 12

Final state of the stack:

Top -> 2
3
Bottom -> 12

Question No: 47 (Marks: 05)

Make the function table for segment 'd' for the 7-segment display.

Input				Output	Input				Output
A	B	C	D	d	A	B	C	D	d
0	0	0	0	1	1	0	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	1	1	0	1	0	x
0	0	1	1	1	1	0	1	1	x
0	1	0	0	0	1	1	0	0	x
0	1	0	1	1	1	1	0	1	x
0	1	1	0	1	1	1	1	0	x
0	1	1	1	0	1	1	1	1	x

Figure 11.12d Function Table for Segment d

Input				Output	Input				Output
A	B	C	D	Seg. e	A	B	C	D	Seg. e
0	0	0	0	1	1	0	0	0	1
0	0	0	1	0	1	0	0	1	0
0	0	1	0	1	1	0	1	0	x
0	0	1	1	0	1	0	1	1	x
0	1	0	0	0	1	1	0	0	x
0	1	0	1	0	1	1	0	1	x
0	1	1	0	1	1	1	1	0	x
0	1	1	1	0	1	1	1	1	x

Figure 11.12e Function Table for Segment e

Question No: 48 (Marks: 05)

Consider the 2 to 4 decoder and complete the following function table.

Input		Output			
I_1	I_0	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Question No: 49 (Marks: 05)

Consider the following Boolean expression and write the equivalent ABEL expression.
F = AB'C + ABC + BD + CD + A'B'C'

Solution:

ABEL expression:

```
F = A&!B&C#A&B&C#B&D#C&D#!A&!B&!C;
```

One another way you can write:

```
F = (A & !B & C) # (A & B & C) # (B & D) # (C & D) # (!A & !B & !C);
```

How?

Boolean Operations and Boolean Notations

The NOT, AND, OR and XOR operations have special symbols in ABEL as shown in table 21.1

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	$

Table 21.1 ABEL Symbols for logic operations

The standard Boolean notations in terms of ABEL notations are defined in table 20.2. The operators !, &, # and $ have precedence in the order given in table.

Boolean Notation	ABEL Notation
$\overline{A}$	!A
A.B	A&B
A + B	A#B
A ⊕ B	A$B

Table 21.2 Boolean and equivalent ABEL Notations

Boolean Equations:

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end with ';'. Figure 21.6

Boolean expression $F = AB + A\overline{C} + \overline{B}\,\overline{D}$

expression F = A & !B # A & C # !B & !D;

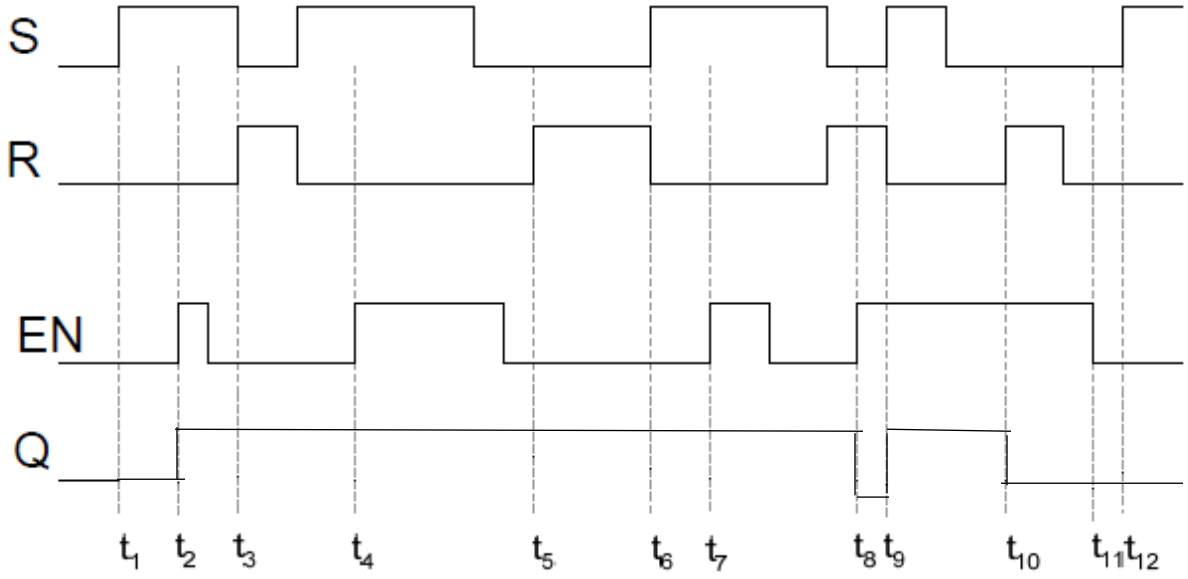
Figure 21.6 ABEL representation of Boolean expression

Consider the Gated S-R Latch and complete the following table

Input			Output
EN	S	R	Q_{t+1}
0	x	X	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	invalid

Question No: 50 (Marks: 05)

Consider the gated S-R latch and draw the output of the following timing diagram



How?

EN	S	R	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	invalid

Table 23.1 Truth-Table of a gated S-R Latch

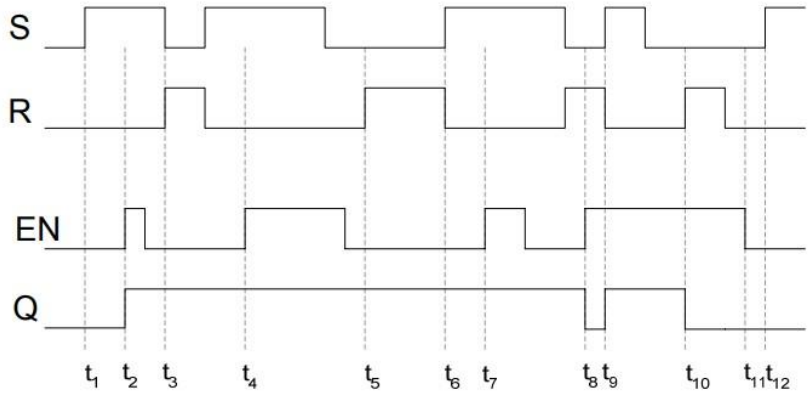


Figure 23.4 Timing diagram of a gated S-R latch