CS302 Final Term Mega File

A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.

► 1

► 2

► 4

► 8

Question No: 2 (M - 1) .

In a sequential circuit the next state is determined by _____ and _____

► State variable, current state

► Current state, flip-flop output

► Current state and external input

► Input and clock signal applied

Question No: 3 (M - 1) .

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► Mod-6, Mod-10

► Mod-50, Mod-10

► Mod-10, Mod-50

► Mod-50, Mod-6

Question No: 4 (M - 1) .

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► True

► False

Question No: 5 (M - 1) .

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

► Set-up time

► Hold time

- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 6 (M - 1) .

74HC163 has two enable input pins which are _____ and _____

- ► ENP, ENT
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

The bolean expression A + BC equals
Select correct option :
(A ' + B)(A ' + C)
(A + B)(A + C)
(A + B)(A' + C)
none of the above

Adjacent 1 s detector circuit will have active high output for the input
Select correct option :
0101
1010
0011
0001

How many data select lines are required for selecting eight inputs ?
Select correct option :
4
3
2
1

Which of the number is not a representative of hexadecimal system
Select correct option :
1234
ABCD
1001
DEFH

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together
Select correct option :
True

False

High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____
Select correct option :
0 . 3 V
0 . 5 V
0 . 9 V
3 . 3 V

To get the answer " 1 " in Boolean addition of three variables , _____
Select correct option :
All three variables must be 1
One of the variables must be 1
All three variables must be 0
Any two variables must be 1

The 3 - variable Karnaugh Map (K- Map) has _____ cells for min or max terms
Select correct option :
4
8
12
16

_____ is invalid number of cells in a single group formed by the adjacent cells in K - map
Select correct option :
2
8
12
16

The boolean expression A + B' + C is
a sum term
a literal term
a product term
a complemented term

Consider A= 1 ,B = 0 , C= 1 . A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____
Select correct option :
Zero
One
Undefined
No output as input is invalid

The Binary number 1011 .101 has an

Integer part represented by _____ and
a fraction part ____ separated by a
decimal point .
Select correct option :
1011, 101
101, 1011
101, 1101
10111, 11

LUT is acronym for _____

- ► Look Up Table
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

. **Question No: 28 (M - 1) .**

The diagram given below represents _____

- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► Sum of product form

Question No: 29 (M - 1) .

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► Doesn’t have an invalid state
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 30 (M - 1) .

A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► Parallel data to serial
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 31 (M - 1) .

A GAL is essentially a _____.

- ► Non-reprogrammable PAL

► PAL that is programmed only by the manufacturer

► Very large PAL

► Reprogrammable PAL

Adding two octal numbers " 36 " and
" 71 " result in _____
Select correct option :
213
123
127
345

The OR Gate performs a Boolean
_____ function
Select correct option :
Addition correct
Subtraction
Multiplication
Division

Adding two octal numbers " 36 " and
" 71 " result in _____
Select correct option :
213
123
127
345

If we multiply " 723 " and " 34 " by
representing them in floating point
notation i .e . by first , converting them
in floating point representation and
then multiplying them, the value of
mantissa of result will be _____
Select correct option :
24 .582
2 . 4582
24582 not sure
0 . 24582

NOR Gate can be used to perform the
operation of AND, OR and NOT Gate
Select correct option :
TRUE
FALSE

The three fundamental gates are

_____
Select correct option :
AND, NAND, XOR
OR , AND, NAND
NOT, NOR , XOR
NOT, OR , AND

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result
Select correct option :
1001
0110
1111
1100

A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values .
Select correct option :
2
4
8
16

In designing any counter the transition from a current state to the next sate is determined by
Select correct option :
Current state and inputs
Only inputs
Only current state
current state and outputs

The 4 - variable K - Map has _____ rows and _____ columns of cells .
Select correct option :
2 , 2
2 , 4
4 , 2
4 , 4NAND gate is form by connecting _____

Select correct option :
AND Gate and then NOT Gate correct
NOT Gate and then AND Gate
AND Gate and then OR Gate
OR Gate and then AND Gate

A standard SOP form has _____ terms that have all the variables in the domain of the expression.
Sum

A synchronous decade counter will have _____ flip - flops
Select correct option :
3
4
7
10

.Which one of the following is not a valid rule of Boolean algebra?
(a) A + 1 = 1
(b) A = Ā
(c) A. A = A
(d) A + 0 = A

How many data select lines are required for selecting eight inputs ?
1
2
3
4

If two adjacent 1 s are detected in the input , the output is set to high .
input combinations will be
0011
0101
1100
1010

The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1. ► Undefined ► One ► Zero ► No Output as input is invalid.

CS302 Question No: 5 (M - 1) **_____ is invalid number of cells in a single group formed by the adjacent cells in K-map.**

► 2 ► 8
► 12 ► 16

CS302 Question No: 6 (M - 1) **The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.** ► AND ► OR ► NOT ► XOR

CS302 Question No: 7 (M - 1) **_____ is one of the examples of synchronous inputs.**
► J-K input
► EN input

► Preset input (PRE)
► Clear Input (CLR)

The 4 - variable Karnaugh Map (K - Map) has _____ rows and ____colums
2 , 2
4 , 4
4 , 2
2 , 4

the boolean expression AB 'CD 'is
a sumterm
a product term
a literal term
always 1

Don’ t care conditions are marked as _____ in the output column of the function table
0
1
X
None of the given options

An example of SOP expression is
A + B (C + D)
A' B + AC ' + AB ' C
(A ' + B + C)(A + B ' + C)
both (a) and (b)

For a Standard SOP expression , a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.
0
1 (ans)
X (don ’ t care condition)

In a 4 - bit binary counter , the next state after the terminal count in the DOWN mode is _____
Select correct option :
0000
1111

0001
10000

A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values .
Select correct option :
2
4
8
16

The OR Gate performs a Boolean _____ function
Select correct option :
Addition
Subtraction
Multiplication
Division

Sum term (Max term) is implemented using _____ gates
Select correct option :
OR
AND
NOT
OR - AND

Above is the circuit diagram of _____.
► Asynchronous up-counter
► Asynchronous down-counter
► Synchronous up-counter
► Synchronous down-counter

CS302 Question No: 26 (M - 1) **The sequence of states that are implemented by a n-bit Johnson counter is**
► n+2 (n plus 2) ► 2n (n multiplied by 2) ► 2n (2 raise to power n) ► n2 (n raise to power 2)

The number " 1259" may belong to _____ number system .
Select correct option :
Binary number system
Octal or Decimal system .
Decimal or Hexadecimal system
Binary or Hexadecimal system

“ 1101 ” in signed representation is equivalent to _____
Select correct option :
10
13
- 10
- 5

TTL based devices work with a dc supply of ____ Volts
Select correct option :
+ 10
+ 5
+ 3
3 . 3

In decimal value “ 275 ” the weight of the digit “ 7 ” is _____
Select correct option :
0
1
10
100

The decimal “ 10 ” will have an octal equivalent _____
Select correct option :
9
10
11
12

Caveman number system is Base _____ number system
Select correct option :
2
5
10
16

The terminal count of a 4 - bit binary counter in the DOWN mode is_ _____
Select correct option :
0000
0011
1100
1111

A divide- by- 10 ring counter requires a minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz
125 KHz
8 MHz

To parallel load a byte of data into a shift register , there must be
Select correct option :
one clock pulse
one clock pulse for each 1 in the data
eight clock pulse
one clock pulse for each 0 in the data

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

With a 100 KHz clock frequency , eight bits can be serially entered into a shift register in
Select correct option :
80 micro seconds
8 micro seconds
80 mili seconds
10 micro seconds

1011+ 101 = _____
Select correct option :
10000
00001
10011
11001

Once the state diagram is drawn for any sequential circuit the next step is to draw
Select correct option :
Transiation table
Karnaugh map
Next- state table
Logic expression

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz Not Confirm
125 KHz
8 MHz

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the DOWN mode is :
Select correct option :
0001
1000
1110
1111

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

Number of states in an 8 - bit Johnson counter sequence are :
Select correct option :
8
12
14
16

In a 4 - bit binary counter , the next state after the terminal count in the DOWN mode is _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Select correct option :
0000
1111
0001
10000

Divide - by- 32 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
DIV 16 and DIV 32

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the UP mode is
Select correct option :
0001
1000
1110
1111

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100
1000
10000

The first Least Most digit in decimal number system has
Select correct option :
Has position 0 and weight equal to 1
not sure
Has position 1 and weight equal to 0
Has position 1 and weight equal to 10
Has position 0 and weight equal to 10

A stage in the shift register consists of
Select correct option :
a latch
a flip flop
a byte of storage
four bits of storage

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz not confirm
125 KHz
8 MHz

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001
1011
0011
1100

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

Three cascaded modulus - 10 counters
have an overall modulus of
Select correct option :
30
100
1000
10000

Question No: 4 (M - 1) .

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

► Using a single comparator

► Using Iterative Circuit based Comparators

► Connecting comparators in vertical hierarchy

► Extra logic gates are always required.

Question No: 5 (M - 1) .

Demultiplexer is also called

► Data selector

► Data router

► Data distributor

► Data encoder

Question No: 6 (M - 1) .

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► Doesn't have an invalid state

► Sets to clear when both J = 0 and K = 0

► It does not show transition on change in pulse

► It does not accept asynchronous inputs

Question No: 7 (M - 1) .

A positive edge-triggered flip-flop changes its state when _____

► Low-to-high transition of clock

► High-to-low transition of clock

► Enable input (EN) is set

► Preset input (PRE) is set

A divide- by- 10 ring counter requires a minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

Number of states in an 8 - bit Johnson counter sequence are :
Select correct option :
8
12
14
16

the terminal count of a modulus - 13 binary counter is
Select correct option :
0000
1111
1101
1100

A Divide - by- 20 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
Div 10 and DIV 16

To serially shift a byte of data into a shift register , there must be
Select correct option :
one clock pulse
one load pulse
eight clock pulses
one clock pulse for each 1 in the data

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

1
A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100
1000
10000

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the DOWN mode is :
Select correct option :
0001
1000
1110
1111

A divide- by- 10 ring counter requires a minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

A multiplexer with a register circuit converts
Select correct option :
Serial data to parallel
Parallel data to serial
Serial data to serial
Parallel data to parallel

In designing any counter the transition from a current state to the next sate is determined by
Select correct option :
Current state and inputs
Only inputs
Only current state
current state and outputs

A decade counter can be implemented

by truncating the counting sequence of a MOD - 20 counter .
Select correct option :
True
False

The terminal count of a 4 - bit binary counter in the DOWN mode is_ _____
Select correct option :
0000
0011
1100
1111

An Asynchronous Down - counter is implemented (Using J - K flip - flop) by connecting _____
Select correct option :
output of all flip - flops to clock input of next flip - flops
output of all flip - flops to clock input of next flip - flops
output of all flip - flops to J input of next flip - flops
output of all flip - flops to K input of next flip - flops

the terminal count of a modulus - 13 binary counter is
Select correct option :
0000
1111
1101
1100

A decade counter can be implemented by truncating the counting sequence of a MOD - 20 counter .
Select correct option :
True
False

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001
1011

0011
1100

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

The glitches due to " Race Condition" can be avoided by using a _____
Select correct option :
Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative - Edge triggered flip - flops

Karnaugh map is used in designing
Select correct option :
a clock
a counter
an UP /DOWN counter
All of the above

_____ is said to occur when multiple internal variables change due to change in one input variable
Select correct option :
Hold and Wait
Clock Skew
Race condition
Hold delay

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100

1000
10000

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

The glitches due to " Race Condition" can be avoided by using a _____
Select correct option :
Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative - Edge triggered flip - flops

A flip - flop is presently in SET stae and must remain SET on the next cliock pulse . What must j and K be ?
Select correct option :
J = 1 , K = 0
J = 1 , K = X (Don't care)
J = X(Don't care), K = 0
J = 0 , K = X (Don't care)

The Synchronous counters are also known as Ripple Counters :
Select correct option :
True
False

The Synchronous counters are also known as Ripple Counters :

Select correct option :
True
False

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

_____ Counters as the name indicates are not triggered simultaneously
Select correct option
Asynchronous
Synchronous
Positive - Edge triggered
Negative- Edge triggered

Ripple Clock Output
The 74 HC 163 is a 4 - bit Synchronous Counter .it has . ...data output pins
Select correct option :
2
4
6
8

A counter is implemented using three (3) flip - flops , possibly it will

have _____ maximum output status .
Select correct option :
3
7
8
15

Sum term (Max term) is implemented using _____ gates
Select correct option :
OR
AND
NOT
OR - AND

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

Divide - by- 32 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by the formula . (“n ” represents the total number of flip - flops)
Select correct option :
(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001
1011
0011
1100

A 4 - bit binary UP / DOWN counter is in the binary state zero . the next state in the DOWN mode is_ _____
Select correct option :
0001
1111
1000
1110

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

A counter is implemented using three (3) flip - flops , possibly it will have _____ maximum output status .
Select correct option :
3
7
8
15

RCO stands for _____
Select correct option :
Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

For a down counter that counts from (111 to 000), if current state is " 101 " the next state will be _____
Select correct option :
111
110
010
none of given options

A Divide - by- 20 counter can be

acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
Div 10 and DIV 16

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

_____ is one of the examples of asynchronous inputs.
- ► J-K input
- ► S-R input
- ► D input
- ► Clear Input (CLR)

CS302 Question No: 9 (M - 1) **The _____ input overrides the _____ input.**
► Asynchronous, synchronous ► Synchronous, asynchronous ► Preset input (PRE), Clear input (CLR) ► Clear input (CLR), Preset input (PRE)

CS302 Question No: 10 (M - 1) **_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.** ► Race condition ► Clock Skew ► Ripple Effect ► None of given options

CS302 Question No: 11 (M - 1) **Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____**
- ► 0000
- ► 1101
- ► 1011
- ► 1111

CS302 Question No: 12 (M - 1) **In a state diagram, the transition from a current state to the next state is determined by** ► Current state and the inputs ► Current state and outputs ► Previous state and inputs ► Previous state and outputs

CS302 Question No: 13 (M - 1) **_____ is used to minimize the possible no. of states of a circuit.** ► State assignment ► State reduction ► Next state table ► State diagram

The glitches due to " Race Condition" can be avoided by using a _____
Select correct option :
Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative- Edge triggered flip - flops

A decade counter is _____
Select correct option :
Mod - 3 counter
Mod - 5 counter
Mod - 8 counter
Mod - 10 counter

The terminal count of a 4 - bit binary counter in the DOWN mode is_ _____
Select correct option :
0000
0011
1100
1111

The Synchronous counters are also known as Ripple Counters :
Select correct option :
True
False

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Design of state diagram is one of many steps used to design
Select correct option :
a clock

a truncated counter
an UP /DOWN counter
any counter

12. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
►**True (Page 160)**
►False

13. The device shown here is most likely a _____
►Comparator
►Multiplexer
►**Demultiplexer click here for detail**
►Parity generator

14. The GAL22V10 has ____ inputs
►**22 (Page 195)**
►10
►44
►20

15. A latch retains the state unless
►Power is turned off
►**Input is changed (page 218)**
►Output is changed
►Clock pulse is changed

16. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.
►**SET (Page 220)**

►RESET
►Clear
►Invalid

17. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (VoH) will be in the range of _____ volts.
►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

18. A.(B.C) = (A.B).C is an expression of _____
►Demorgan‟s Law

►Distributive Law
►Commutative Law
►**Associative Law (Page 72)**

In a 4 - bit binary counter , the next state after the terminal count in the DOWN mode is _____
Select correct option :
0000
1111
0001
10000

A 5 - variable karnaugh map has
Select correct option :
sixteen cells
thirty two cells
sixty- four cells
None of these

The bolean expression A + BC equals
Select correct option :
(A ' + B)(A' + C)
(A + B) (A + C)
(A + B) (A ' + C)
none of the above

the boolean expression AB 'CD 'is
Select correct option :
a sumterm
a product term
a literal term
always 1

The OR Gate performs a Boolean _____ function
►**Addition (Page 42)**
►Subtraction
►Multiplication
►Division

4. TTL based devices work with a dc supply of ____ Volts
►+10
►**+5 (Page 61)**
►+3
►3.3

5. A standard POS form has _____ terms that have all the variables in the domain of the expression.
►**Sum (Page 85)**
►Product

►Min
►Composite

6. A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.
►2
►4
►**8 (According to rule)**
►16

7. A BCD to 7-Segment decoder has
►3 inputs and 7 outputs
►**4 inputs and 7 outputs (Page 103)**
►7 inputs and 3 outputs
► inputs and 4 outputs

8. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?
►A
►
►**C click here for detail**
►D
9. The binary value of 1010 is converted to the product term
►True
►**False**

Which one of the following is NOT a valid rule of Boolean algebra?
Select correct option :
A + 1 = 1
A = A '
AA = A
A + 0 = A

In a 4 - variable K - map , a 2 - variable product term is produced by
Select correct option :
a 2 - cell group of 1 s
a 8 - cell group of 1 s
a 4 - cell group of 1 s
a 4 - cell group of 0 s

On a Karnaugh map , grouping the 0 s produces
Select correct option :
a POS expression
a SOP expression
a " don ' t care " condition

AND- OR logic

A 3 - variable karnaugh map has
Select correct option :
eight cells
three cells
sixteen cells
four cells

which of the following rules states that if one input of an AND gate is always 1 , the output is equal to the other input ?
Select correct option :
A + 1 = 1
A + A = A
A. A = A
A. 1 = A

2 ' s complement of 5 is
Select correct option :
1101
1011
0101
1100

An example of SOP expression is
Select correct option :
A + B (C + D)
A' B + AC ' + AB ' C
(A ' + B + C)(A + B ' + C)
both (a) nad (b)

2's complement of any binary number can be calculated by
► adding 1's complement twice
► adding 1 to 1's complement (Page 144)
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____
► 86 (According to formula)
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.
► AND
► OR
► NOT

► XOR (Page 186)

MIDTERM EXAMINATION 2010

1. The binary value "11011" is equivalent to _____
►1B (According to rule)
►1C
►1D
►1E

2. An important application of AND Gate is its use in counter circuit
►True (Page 281)
►False

Adjacent 1 s detector circuit will have
active low output for the input
Select correct option :
1101
1010 (Not Confirm)
0110
1011

The complement of a variable is always
Select correct option :
0
1
equal to the variable
the inverse of the variable

Adjacent 1 s detector circuit will have
active high output for the input
Select correct option :
0101
1010
0011
0001

The domain of the expression AB 'CD +
AB ' + C 'D + B is
Select correct option :
A and D
B only
A, B, C and D
none of these

the boolean expression A + B ' + C is
Select correct option :
a sum term
a literal term

a product term
a complemented term

The boolean expression (A + C) (AB ' +
AC) (A 'C ' + B ') can be simplified to
Select correct option :
AB '
AB + A' C
A' B + BC
AB + BC

The boolean expression X = AB + CD
represents
Select correct option :
two ORs ANDed together
a 4 - input AND gate
two ANDs ORed together
an exclusive - Or

Which one of the following is NOT a
valid rule of Boolean algebra?
Select correct option :
A + 1 = 1
A = A '
AA = A
A + 0 = A
The function to be performed by the processor is selected by set of inputs known as _____
► **Function Select Inputs (Page 147)**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.
► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____
► Demorgan‟s Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

How many data select lines are
required for selecting eight inputs ?
Select correct option :
4
3
2
1

the boolean expression AB 'CD 'is
a sumterm
a product term
a literal term
always 1

The boolean expression (A + C) (AB'
+AC) (A 'C ' + B ') can be simplified to
AB '
AB + A 'C
A' B + BC
AB + BC

which of the following rules states
that if one input of an AND gate is
always 1 , the output is equal to the
other input ?
A + 1 =1
A + A = A
A. A = A
A .1 = A

The range of Excess-8 code is from _____ to _____
► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____
►
►
AA =□0 **(Page 85)**
►
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
► 4
► **8 (Page 89)**
► 12
► 16

1) The terminal count of a 4-bit binary counter in the UP mode is----------.

Ans. 1100 or (1111) (not sure which one is correct)

2) For a down counter that counts from (111 to 000). If current state is "101" the next state will be----------.

a) 111

b) 110

c) 010

d) none of given options

3) The n Flip-Flops store---------- states.

Ans. 2^n

4) As Asynchronous Down-counter is implemented (using j-k flip-flop) by connecting----------.

Ans. Q output of all flip-flop to clock input of next flip-flops

5) In case of cascading integrated circuit counters, the enable inputs and RCO of the integrated Circuit counters allow cascading of multiple counters together.

Ans. True

6) The 7HC163 is a 4-bit synchronous counter. It has ---------- data outputs pins.

Ans. 4

7) ---------- Counters as the name indicates are not triggered simultaneously.

Ans. Asynchronous

8) Divide by-32 counter can be achieved by using:

Ans. Flip-flop and DIV 16

9) The --------- input overrides the ---------- input.

Ans. Asynchronous, synchronous

10) A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

Ans. False

11) A mono-stable device only has a single stable state.

Ans. True

12) The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the----------.

Ans. Set-up time

13) The low to high or high to low transition of the clock is considered to be a(n)----------.

Ans. edge

14) The 74HC163 is a 4-bit Synchronous Counter. It has ---------- parallel data input pins.

Ans. 4

15) A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state on the next clock pulse, to what state does the counter go?

Ans. 1001 or (1011) (not sure which one is correct)

16) When the ---------- Hz sampling interval is selected, the signal at the output of the j-k flip-flop has a time period of ---------- seconds.

Ans. 1,2

17) Assume a J-K flip-flop has 1s on the j and k inputs. The next clock pulse will cause the output to----------.

Ans. Toggle

18) The 3-bit up counter can be implemented using ----------.

Ans. S-R flip-flops and D flip-flops

Karnaugh map is used in designing

All of the above

In Master-Slave flip-flop setup, the master flip flop operates at _____

Both Master-Slave operate simultaneously

When the both inputs of edge-triggered J-K flop-flop are set to logic zero _____

Q=0 and Q'=1

To implement the counter using S-R flip-flops instead of J-K flip-flops, the _____ transition table is used.

S-R

The 3-bit up counter can be implemented using _____ flip-flop(s).

S-R Flip-flips and D-Flip-flops

The _____ inputs can be directly mapped to Karnaugh maps.

J-K

Design of state diagram is one of many steps used to design

any counter

In moore machine the output depends on

the current state

A positive edge-triggered flip-flop changes its state when _____

Low-to-high transition of clock

An Astable multivibrator is known as a(n) _____

Oscillator

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Question No: 1 (Marks: 1) - Please choose one
A solution is said to be efficient if it solves the problem within its resource constraints i.e. hardware and time.
- ► **True (Page 4)**
- ► False

Question No: 2 (Marks: 1) - Please choose one
Which one of the following is known as "Last-In, First-Out" or LIFO Data Structure?
- ► Linked List
- ► **Stack (Page 54)**
- ► Queue
- ► Tree

Question No: 3 (Marks: 1) - Please choose one
What will be postfix expression of the following infix expression?
Infix Expression : a+b*c-d
- ► ab+c*d-
- ► **abc*+d-**
- ► abc+*d-
- ► abcd+*-

Question No: 4 (Marks: 1) - Please choose one
For compiler a postfix expression is easier to evaluate than infix expression?
- ► **True Click here for detail**
- ► False

Question No: 5 (Marks: 1) - Please choose one
Consider the following pseudo code
declare a stack of characters
while (there are more characters in the word to read)
{

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```
    read a character
    push the character on the stack
  }
  while ( the stack is not empty )
  {
    pop a character off the stack
    write the character to the screen
  }
```

What is written to the screen for the input "apples"?

- ► selpa
- ► **selppa**
- ► apples
- ► aaappppplleess

Question No: 6 (Marks: 1) - Please choose one

Consider the following function:

```
void test_a(int n)
{
      cout << n << " ";
      if (n>0)
      test_a(n-2);
}
```

What is printed by the call test_a(4)?

- ► **4 2**
- ► 0 2 4
- ► 0 2
- ► 2 4

Question No: 7 (Marks: 1) - Please choose one

If there are N external nodes in a binary tree then what will be the no. of internal nodes in this binary tree?

- ► **N -1 (Page 304)**
- ► N+1
- ► N+2
- ► N

Question No: 8 (Marks: 1) - Please choose one

If there are N internal nodes in a binary tree then what will be the no. of external nodes in this binary tree?

- ► N -1
- ► N
- ► **N +1 (Page 303)**
- ► N +2

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Question No: 9 (Marks: 1) - Please choose one

If we have 1000 sets each containing a single different person. Which of the following relation will be true on each set:

- **Reflexive (page 387)**
- Symmetric
- Transitive
- Associative

Question No: 10 (Marks: 1) - Please choose one

Which one of the following is NOT the property of equivalence relation:

- Reflexive
- Symmetric
- Transitive
- **Associative (page 387)**

Question No: 11 (Marks: 1) - Please choose one

A binary tree of N nodes has _____.

- Log_{10} N levels
- **Log_2 N levels (Page 212)**
- N / 2 levels
- N x 2 levels

Question No: 12 (Marks: 1) - Please choose one

The easiest case of deleting a node from BST is the case in which the node to be deleted _____.

- **Is a leaf node (Page 173)**
- Has left subtree only
- Has right subtree only
- Has both left and right subtree

Question No: 13 (Marks: 1) - Please choose one

If there are N elements in an array then the number of maximum steps needed to find an element using Binary Search is _____ .

- N
- N^2
- $Nlog_2N$
- **log_2N (page 440)**

Question No: 14 (Marks: 1) - Please choose one

Merge sort and quick sort both fall into the same category of sorting algorithms. What is this category?

- O(nlogn) sorts
- Interchange sort (not sure)
- Average time is quadratic
- **None of the given options. (Page 488)**

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Question No: 15 (Marks: 1) - Please choose one
If one pointer of the node in a binary tree is NULL then it will be a/an _____ .

- ► **External node (Page 303)**
- ► Root node
- ► Inner node
- ► Leaf node

Question No: 16 (Marks: 1) - Please choose one
We convert the _____ pointers of binary to threads in threaded binary tree.

- ► Left
- ► Right
- ► **NULL (Page 312)**
- ► None of the given options

Question No: 17 (Marks: 1) - Please choose one
If the bottom level of a binary tree is NOT completely filled, depicts that the tree is NOT a

- ► Expression tree
- ► Threaded binary tree
- ► **complete Binary tree (Page 323)**
- ► Perfectly complete Binary tree

Question No: 18 (Marks: 1) - Please choose one
What is the best definition of a *collision* in a hash table?

- ► Two entries are identical except for their keys.
- ► Two entries with different data have the exact same key
- ► **Two entries with different keys have the same exact hash value. (page 464)**
- ►Two entries with the exact same key have different hash values.

Question No: 19 (Marks: 1) - Please choose one
Suppose that a selection sort of 100 items has completed 42 iterations of the main loop. How many items are now guaranteed to be in their final spot (never to be moved again)

- ► 21
- ► 41
- ► **42** **Click here for detail**
- ► 43

Question No: 20 (Marks: 1) - Please choose on
Suppose you implement a Min heap (with the smallest element on top) in an array. Consider the different arrays below; determine the one that *cannot* possibly be a heap:

- ► 16, 18, 20, 22, 24, 28, 30
- ► 16, 20, 18, 24, 22, 30, 28
- ► 16, 24, 18, 28, 30, 20, 22
- ► **16, 24, 20, 30, 28, 18, 22 (page 334)**

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Question No: 21 (Marks: 1) - Please choose one

Do you see any problem in the code of nextInOrder below:

```
TreeNode * nextInorder(TreeNode * p)
{
  if(p->RTH == thread)
    return( p->R );
  else {
    p = p->R;
  while(p->LTH == child)
 p = p->R;
  return p;
  }
}
```

► The function has no problem and will fulfill the purpose successfully.
► The function cannot be compile as it has syntax error.
► The function has logical problem, therefore, it will not work properly.
► The function will be compiled but will throw runtime exception immediately after the control is transferred to this function.

Question No: 22 (Marks: 1) - Please choose one

Which of the following statement is correct about find(x) operation:

► A find(x) on element x is performed by returning exactly the same node that is found.
► A find(x) on element x is performed by returning the root of the tree containing x. Click here for detail
► A find(x) on element x is performed by returning the whole tree itself containing x.
► A find(x) on element x is performed by returning TRUE.

Question No: 23 (Marks: 1) - Please choose on

Which of the following statement is NOT correct about find operation:

► It is not a requirement that a find operation returns any specific name, just that finds on two elements return the same answer if and only if they are in the same set.
► One idea might be to use a tree to represent each set, since each element in a tree has the same root, thus the root can be used to name the set.
► Initially each set contains one element.
► Initially each set contains one element and it does not make sense to make a tree of one node only.

Question No: 24 (Marks: 1) - Please choose one

In complete binary tree the bottom level is filled from _____

► Left to right (Page 323)
► Right to left
► Not filled at all
► None of the given options

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Question No: 25 (Marks: 1) - Please choose one

Here is an array of ten integers:

5 3 8 9 1 7 0 2 6 4

The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest to largest).

- **► 0 3 8 9 1 7 5 2 6 4 (Page 477)**
- ► 2 6 4 0 3 8 9 1 7 5
- ► 2 6 4 9 1 7 0 3 8 5
- ► 0 3 8 2 6 4 9 1 7 5

Question No: 26 (Marks: 1) - Please choose one

What requirement is placed on an array, so that *binary search* may be used to locate an entry?

- ► The array elements must form a heap.
- ► The array must have at least 2 entries.
- **► The array must be sorted.** **Click here for detail**
- ► The array's size must be a power of two

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Question No: 1 (Marks: 1) - Please choose one

Which one of the following operations returns top value of the stack?

- ► Push
- ► Pop
- **► Top (page 53)**
- ► First

Question No: 2 (Marks: 1) - Please choose one

Compiler uses which one of the following in Function calls,

- **► Stack (page 80)**
- ► Queue
- ► Binary Search Tree
- ► AVL Tree

Question No: 3 (Marks: 1) – Please choose one

Every AVL is _____

- ► Binary Tree
- ► Complete Binary Tree
- ► None of these
- **► Binary Search Tree** **Click here for detail**

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Question No: 4 (Marks: 1) – Please choose one

If there are 56 internal nodes in a binary tree then how many external nodes this binary tree will have?

- ► 54
- ► 55
- ► 56
- ► **57 (page 303)**

Question No: 5 (Marks: 1) - Please choose one

If there are 23 external nodes in a binary tree then what will be the no. of internal nodes in this binary tree?

- ► 23
- ► 24
- ► 21
- ► **22 (page 303)**

Question No: 6 (Marks: 1) - Please choose one

Which one of the following is not an example of equivalence relation?

- ► Electrical connectivity
- ► Set of people
- ► **<= relation (page 388)**
- ► Set of pixels

Question No: 7 (Marks: 1) - Please choose one

Binary Search is an algorithm of searching, used with the _____ data.

- ► **Sorted (page 432)**
- ► Unsorted
- ► Heterogeneous
- ► Random

Question No: 8 (Marks: 1) - Please choose one

Which one of the following is NOT true regarding the skip list?

- ► Each list S_i contains the special keys + infinity and - infinity.
- ► List S_0 contains the keys of S in non-decreasing order.
- ► Each list is a subsequence of the previous one.
- ► **List S_h contains only the n special keys. (page 446)**

Question No: 9 (Marks: 1) - Please choose one

A simple sorting algorithm like selection sort or bubble sort has a worst-case of

- ► O(1) time because all lists take the same amount of time to sort
- ► O(n) time because it has to perform n swaps to order the list.
- ► **$O(n^2)$ time because sorting 1 element takes O(n) time - After 1 pass through the list,either of these algorithms can guarantee that 1 element is sorted. (page 487)**
- ► $O(n^3)$ time, because the worst case has really random input which takes longer to sort.

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Question No: 10 (Marks: 1) - Please choose one
Which of the following is a property of binary tree?
- ► A binary tree of N external nodes has N internal node.
- ► **A binary tree of N internal nodes has N+ 1 external node. (page 303)**
- ► A binary tree of N external nodes has N+ 1 internal node.
- ► A binary tree of N internal nodes has N- 1 external node.

Question No: 11 (Marks: 1) - Please choose one
By using _____we avoid the recursive method of traversing a Tree, which makes use of stacks and consumes a lot of memory and time.
- ► Binary tree only
- ► **Threaded binary tree (page 306)**
- ► Heap data structure
- ► Huffman encoding

Question No: 12 (Marks: 1) - Please choose one
Which of the following statement is true about dummy node of threaded binary tree?
- ► This dummy node never has a value.
- ► This dummy node has always some dummy value.
- ► **This dummy node has either no value or some dummy value. (Page 321)**
- ► This dummy node has always some integer value.

Question No: 13 (Marks: 1) - Please choose one
For a perfect binary tree of height h, having N nodes, the sum of heights of nodes is
- ► N – (h – 1)
- ► **N – (h + 1) (page 373)**
- ► N – 1
- ► N – 1 + h

Question No: 14 (Marks: 1) - Please choose one
What is the best definition of a *collision* in a hash table?
- ► Two entries are identical except for their keys.
- ► Two entries with different data have the exact same key
- ► **Two entries with different keys have the same exact hash value. (page 464)**
- ► Two entries with the exact same key have different hash values.

Question No: 15 (Marks: 1) - Please choose one
Which formula is the best approximation for the depth of a heap with n nodes?
- ► **log (base 2) of n (page 353)**
- ► The number of digits in n (base 10), e.g., 145 has three digits
- ► The square root of n
- ► n

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Question No: 16 (Marks: 1) - Please choose one

Which of the following statement is NOT correct about find operation:

► It is not a requirement that a find operation returns any specific name, just that finds on two elements return the same answer if and only if they are in the same set.

► One idea might be to use a tree to represent each set, since each element in a tree has the same root, thus the root can be used to name the set.

► Initially each set contains one element.

► **I**nitiall**y** each set contains one element and it does not make sense to make a tree of one node only.

Question No: 17 (Marks: 1) - Please choose one

Which of the following is not true regarding the maze generation?

► Randomly remove walls until the entrance and exit cells are in the same set.

► Removing a wall is the same as doing a union operation.

► Remove a randomly chosen wall if the cells it separates are already in the same set. (page 424)

► Do not remove a randomly chosen wall if the cells it separates are already in the same set.

Question No: 18 (Marks: 1) – Please choose one

In threaded binary tree the NULL pointers are replaced by ,

► preorder successor or predecessor

► inorder successor or predecessor (page 307)

► postorder successor or predecessor

► NULL pointers are not replaced

Question No: 19 (Marks: 1) - Please choose one

Which of the given option is NOT a factor in Union by Size:

► Maintain sizes (number of nodes) of all trees, and during union.

► Make smaller tree, the subtree of the larger one.

► Make the larger tree, the subtree of the smaller one. (page 408)

► Implementation: for each root node i, instead of setting parent[i] to -1, set it to -k if tree rooted at i has k nodes.

Question No: 20 (Marks: 1) - Please choose one

Suppose we had a hash table whose hash function is “n % 12”, if the number 35 is already in the hash table, which of the following numbers would cause a collision?

► 144

► 145

► **143**

► 148

Question No: 21 (Marks: 1) - Please choose o

What requirement is placed on an array, so that *binary search* may be used to locate an entry?

► The array elements must form a heap.

► The array must have at least 2 entries.

► The array must be sorted. Click here for detail

► The array’s size must be a power of two

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Question No: 22 (Marks: 1) - Please choose one
A binary tree with 24 internal nodes has _____ external nodes.

- ► 22
- ► 23
- ► 48
- ► **25 (page 303)**

Question No: 23 (Marks: 1) - Please choose on
In case of deleting a node from AVL tree, rotation could be prolong to the *root* node.

- ► **Yes (Page 267)**
- ► No

Question No: 24 (Marks: 1) - Please choose one
when we have declared the size of the array, it is not possible to increase or decrease it during the _____of the program.

- ► Declaration
- ► **Execution (page 17)**
- ► Defining
- ► None of the abov

Question No: 25 (Marks: 1) - Please choose one
it will be efficient to place stack elements at the start of the list because insertion and removal take _____time.

- ► Variable
- ► **Constant (page 60)**
- ► Inconsistent
- ► None of the above

Question No: 26 (Marks: 1) - Please choose one
_____ is the stack characteristic but _____was implemented because of the size limitation of the array.

- ► isFull(),isEmpty()
- ► pop(), push()
- ► **isEmpty() , isFull() (page 59)**
- ► push(),pop()

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Question No: 1 (Marks: 1) - Please choose one
What kind of list is best to answer questions such as "What is the item at position n?"

- ► **Lists implemented with an array.** **Click here for detail**
- ► Doubly-linked lists.
- ► Singly-linked lists.
- ► Doubly-linked or singly-linked lists are equally best

Question No: 2 (Marks: 1) - Please choose one
Each node in doubly link list has,

- ► 1 pointer
- ► **2 pointers (page 39)**
- ► 3 pointers
- ► 4 pointers

Question No: 3 (Marks: 1) - Please choose one
If there are 56 internal nodes in a binary tree then how many external nodes this binary tree will have?

- ► 54
- ► 55
- ► 56
- ► **57 (page 303)**

Question No: 4 (Marks: 1) - Please choose one
If there are N internal nodes in a binary tree then what will be the no. of external nodes in this binary tree?

- ► N -1
- ► N
- ► **N +1 (page 303)**
- ► N +2

Question No: 5 (Marks: 1) - Please choose one
A binary tree with N internal nodes has _____ links, _____ links to internal nodes and _____ links to external nodes

- ► N+1, 2N, N-1
- ► N+1, N-1, 2N
- ► **2N, N-1, N+1 (page 304)**
- ► N-1, 2N, N+1

Question No: 6 (Marks: 1) - Please choose one
The definition of Transitivity property is

- ► For all element x member of S, x R x
- ► For all elements x and y, x R y if and only if y R x
- ► **For all elements x, y and z, if x R y and y R z then x R z (page 385)**
- ► For all elements w, x, y and z, if x R y and w R z then x R z

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Question No: 7 (Marks: 1) - Please choose one
Which one of the following is not an example of equivalence relation:

- ► Electrical connectivity
- ► Set of people
- ► **<= relation (page 388)**
- ► Set of pixels

Question No: 8 (Marks: 1) - Please choose one
Union is a _____ time operation.

- ► **Constant (page 405)**
- ► Polynomial
- ► Exponential
- ► None of the given options

Question No: 9 (Marks: 1) - Please choose one
Binary Search is an algorithm of searching, used with the _____ data.

- ► **Sorted (page 432)**
- ► Unsorted
- ► Heterogeneous
- ► Random

Question No: 10 (Marks: 1) - Please choose one
A simple sorting algorithm like selection sort or bubble sort has a worst-case of

- ► O(1) time because all lists take the same amount of time to sort
- ► O(n) time because it has to perform n swaps to order the list.
- ► **$O(n^2)$ time because sorting 1 element takes O(n) time - After 1 pass through the list, either of these algorithms can guarantee that 1 element is sorted. (page 487)**
- ► $O(n^3)$ time, because the worst case has really random input which takes longer to sort.

Question No: 11 (Marks: 1) - Please choose one
Merge sort and quick sort both fall into the same category of sorting algorithms. What is this category?

- ► O(nlogn) sorts
- ► Interchange sort
- ► Average time is quadratic
- ► **None of the given options. (Page 488)**

Question No: 12 (Marks: 1) - Please choose one
Huffman encoding uses _____ tree to develop codes of varying lengths for the letters used in the original message.

- ► Linked list
- ► Stack
- ► Queue
- ► **Binary tree (page 287)**

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Question No: 13 (Marks: 1) - Please choose one

Which of the following statement is true about dummy node of threaded binary tree?

► The left pointer of dummy node points to the itself while the right pointer points to the root of tree.

► **The left pointer of dummy node points to the root node of the tree while the right pointer points itself i.e. to *dummy* node (page 321)**

► The left pointer of dummy node points to the root node of the tree while the right pointer is always NULL.

► The right pointer of dummy node points to the itself while the left pointer is always NULL.

Question No: 14 (Marks: 1) - Please choose one

Consider a min heap, represented by the following array:
10,30,20,70,40,50,80,60
After inserting a node with value 31.Which of the following is the updated min heap?

► **10,30,20,31,40,50,80,60,70 (page 336)**

► 10,30,20,70,40,50,80,60,31

► 10,31,20,30,40,50,80,60,31

► 31,10,30,20,70,40,50,80,60

Question No: 15 (Marks: 1) - Please choose one

Consider a min heap, represented by the following array:
11,22,33,44,55
After inserting a node with value 66.Which of the following is the updated min heap?

► **11,22,33,44,55,66 (page 336)**

► 11,22,33,44,66,55

► 11,22,33,66,44,55

► 11,22,66,33,44,55

Question No: 16 (Marks: 1) - Please choose one

Suppose that a selection sort of 100 items has completed 42 iterations of the main loop. How many items are now guaranteed to be in their final spot (never to be moved again)?

► 21

► 41

► **42** **Click here for detail**

► 43

Question No: 17 (Marks: 1) - Please choose one

_____ is a data structure that can grow easily dynamically at run time without having to copy existing elements.

► Array ()

► List

► **Both of these (page 10)**

► None of these

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Question No: 18 (Marks: 1) - Please choose one
The maximum number of external nodes (leaves) for a binary tree of height H is _____

► **2^H** **Click here for detail**
► 2^H+1
► 2^H-1
► 2^H+2

Question No: 19 (Marks: 1) - Please choose one
A complete binary tree of height ____ has nodes between 16 to 31 .

► 2
► 3
► **4 (page 373)**
► 5

Question No: 20 (Marks: 1) - Please choose one
Which of the given option is NOT a factor in Union by Size:

► Maintain sizes (number of nodes) of all trees, and during union.
► Make smaller tree, the subtree of the larger one.
► **Make the larger tree, the subtree of the smaller one. (page 408)**
► Implementation: for each root node i, instead of setting parent[i] to -1, set it to -k if tree rooted at i has k nodes.

Question No: 21 (Marks: 1) - Please choose one
Here is an array of ten integers:

5 3 8 9 1 7 0 2 6 4

The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest to largest).

► 0 3 8 9 1 7 5 2 6 4 **(Page 477)**
► 2 6 4 0 3 8 9 1 7 5
► 2 6 4 9 1 7 0 3 8 5
► 0 3 8 2 6 4 9 1 7 5

Question No: 22 (Marks: 1) - Please choose one
Suppose A is an array containing numbers in increasing order, but some numbers occur more than once when using a binary search for a value, the binary search always finds _____

► **the first occurrence of a value.** **Click here for detail**
► the second occurrence of a value.
► may find first or second occurrence of a value.
► None of the given options.

Question No: 23 (Marks: 1) - Please choose one
A binary tree with 24 internal nodes has _____ external nodes.

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► 22
► 23
► 48
► **25 (page 303)**

Question No: 24 (Marks: 1) - Please choose one
it will be efficient to place stack elements at the start of the list because insertion and removal take _____time.

► Variable
► **Constant (page 60)**
► Inconsistent
► None of the above

Question No: 25 (Marks: 1) - Please choose one
"+" is a _____operator.

► Unary
► **Binary (page 64)**
► Ternary
► None of the above

Question No: 26 (Marks: 1) - Please choose one
A kind of expressions where the operator is present between two operands called _____expressions.
► Postfix
► **Infix (page 64)**
► Prefix
► None of the above.

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
Here is a small function definition:

```
void f(int i, int &k)
{
i = 1;
k = 2;
}
```

Suppose that a main program has two integer variables x and y, which are given the value 0. Then the main program calls f(x,y); What are the values of x and y after the function f finishes?

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► Both x and y are still 0.
► x is now 1, but y is still 0.
► **x is still 0, but y is now 2.**
► x is now 1, and y is now 2.

Question No: 2 (Marks: 1) - Please choose one
A binary tree with N internal nodes has _____ links, _____ links to internal nodes and _____ links to external nodes

► N+1, 2N, N-1
► N+1, N-1, 2N
► **2N, N-1, N+1 (page 304)**
► N-1, 2N, N+1

Question No: 3 (Marks: 1) - Please choose one
Each node in doubly link list has,
► 1 pointer
► **2 pointers (Page 39)**
► 3 pointers
► 4 pointers

Question No: 4 (Marks: 1) - Please choose one
If you know the size of the data structure in advance, i.e., at compile time, which one of the following is a good data structure to use.

► Array
► List
► **Both of these (page 10)**
► None of these

Question No: 5 (Marks: 1) - Please choose one
Which one of the following is not an example of equivalence relation:

► Electrical connectivity
► Set of people
► **<= relation (Page 388)**
► Set of pixels

Question No: 6 (Marks: 1) - Please choose one
If a complete binary tree has height h then its no. of nodes will be,
► Log (h)
► **2^{h+1} - 1 (page 125)**
► Log (h) - 1
► 2^h - 1

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Question No: 7 (Marks: 1) - Please choose one
If a max heap is implemented using a partially filled array called data, and the array contains n elements (n > 0), where is the entry with the greatest value? **Data[0] is correct**

- ► data[1]
- ► data[n-1]
- ► data[n]
- ► data[2*n+1]

Question No: 8 (Marks: 1) - Please choose one
Which one is a self-referential data type?

- ► Stack
- ► Queue
- ► **Link list** **Click here for detail**
- ► All of these

Question No: 9 (Marks: 1) - Please choose one
There is/are _____ case/s for rotation in an AVL tree,

- ► 1
- ► 3
- ► 2
- ► **4 (page 229)**

Question No: 10 (Marks: 1) - Please choose one
Which of the following can be the inclusion criteria for pixels in image segmentation.

- ► Pixel intensity
- ► Texture
- ► Threshold of intensity
- ► **All of the given options (page 421)**

Question No: 11 (Marks: 1) - Please choose one
Consider te following array
23 15 5 12 40 10 7
After the first pass of a particular algorithm, the array looks like
15 5 12 23 10 7 40
Name the algorithm used

- ► Heap sort
- ► Selection sort
- ► Insertion sort
- ► **Bubble sort (According to rule)**

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Question No: 12 (Marks: 1) - Please choose one
In a perfectly balanced tree the insertion of a node needs _____ .

► **One rotation (Page 225)**
► Two rotations
► Rotations equal to number of levels
► No rotation at all

Question No: 13 (Marks: 1) - Please choose one
If there are N elements in an array then the number of maximum steps needed to find an element using Binary Search is _____ .

► N
► N^2
► $Nlog_2N$
► **log_2N (page 440)**

Question No: 14 (Marks: 1) - Please choose one
Which of the following is NOT a correct statement about Table ADT.
► In a table, the type of information in columns may be different.
► **A table consists of several columns, known as entities. (page 408)**
► The row of a table is called a record.
► A major use of table is in databases where we build and use tables for keeping information.

Question No: 15 (Marks: 1) - Please choose one
If both pointers of the node in a binary tree are NULL then it will be a/an _____ .

► Inner node
► **Leaf node (page 120)**
► Root node
► None of the given options

Question No: 16 (Marks: 1) - Please choose one
Suppose we are sorting an array of eight integers using quick sort, and we have just finished the first partitioning with the array looking like this:

2 5 1 7 9 12 11 10

Which statement is correct?

► **The pivot could be either the 7 or the 9.(page 506)**
► The pivot could be the 7, but it is not the 9.
► The pivot is not the 7, but it could be the 9.
► Neither the 7 nor the 9 is the pivot.

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Question No: 17 (Marks: 1) - Please choose one
What is the best definition of a *collision* in a hash table?

► Two entries are identical except for their keys.
► Two entries with different data have the exact same key
► **Two entries with different keys have the same exact hash value. (page 464)**
► Two entries with the exact same key have different hash values.

Question No: 18 (Marks: 1) - Please choose one
For a perfect binary tree of height h, having N nodes, the sum of heights of nodes is

► N – (h – 1)
► **N – (h + 1) (Page 373)**
► N – 1
► N – 1 + h

Question No: 19 (Marks: 1) - Please choose one
A binary tree with 33 internal nodes has _____ links to internal nodes.

► 31
► **32 (Page 304)**
► 33
► 66

Question No: 20 (Marks: 1) - Please choose one
Suppose you implement a Min heap (with the smallest element on top) in an array. Consider the different arrays below; determine the one that *cannot* possibly be a heap:

► 16, 18, 20, 22, 24, 28, 30
► 16, 20, 18, 24, 22, 30, 28
► 16, 24, 18, 28, 30, 20, 22
► **16, 24, 20, 30, 28, 18, 22 (see min heap property at page 337)**

Question No: 21 (Marks: 1) - Please choose one
Which of the following is not true regarding the maze generation?

► Randomly remove walls until the entrance and exit cells are in the same set.
► Removing a wall is the same as doing a union operation.
► **Remove a randomly chosen wall if the cells it separates are already in the same set. (Page 424)**
► Do not remove a randomly chosen wall if the cells it separates are already in the same set.

Question No: 22 (Marks: 1) - Please choose one
Which formula is the best approximation for the depth of a heap with n nodes?

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► **log (base 2) of n (Page 353)**
► The number of digits in n (base 10), e.g., 145 has three digits
► The square root of n
► n

Question No: 23 (Marks: 1) - Please choose one
In threaded binary tree the NULL pointers are replaced by ,

► preorder successor or predecessor
► **inorder successor or predecessor (Page 307)**
► postorder successor or predecessor
► NULL pointers are not replaced

Question No: 24 (Marks: 1) - Please choose one
The _____ method of list will position the *currentNode* and *lastCurrentNode* at the start of the list.

► Remove
► Next
► **Start (Page 38)**
► Back

Question No: 25 (Marks: 1) - Please choose one
Mergesort makes two recursive calls. Which statement is true after these recursive calls finish, but before the merge step?

► Elements in the first half of the array are less than or equal to elements in the second half of the array.
► None of the given options.
► The array elements form a heap.
► **Elements in the second half of the array are less than or equal to elements in the first half of the array.** **Click here for detail**

Question No: 26 (Marks: 1) - Please choose one
Suppose we had a hash table whose hash function is “n % 12”, if the number 35 is already in the hash table, which of the following numbers would cause a collision?

► 144
► 145
► **143**
► 148

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FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The arguments passed to a function should match in number, type and order with the parameters in the function definition.

► **True**
► False

Question No: 2 (Marks: 1) - Please choose one
If numbers 5, 222, 4, 48 are inserted in a queue, which one will be removed first?

► 48
► 4
► 222
► **5 (According to rule)**

Question No: 3 (Marks: 1) - Please choose one
Suppose currentNode refers to a node in a linked list (using the Node class with member variables called data and nextNode). What statement changes currentNode so that it refers to the next node?

► currentNode ++;
► currentNode = nextNode;
► currentNode += nextNode;
► **currentNode = currentNode->nextNode;**

Question No: 4 (Marks: 1) - Please choose one
A **Compound Data Structure** is the data structure which can have multiple data items of same type or of different types. Which of the following can be considered compound data structure?
► Arrays
► LinkLists
► Binary Search Trees
► **All of the given options** **Click here for detail**

Question No: 5 (Marks: 1) - Please choose one
Here is a small function definition:

```
void f(int i, int &k)
{
i = 1;
k = 2;
}
```

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Suppose that a main program has two integer variables x and y, which are given the value 0. Then the main program calls f(x,y); What are the values of x and y after the function f finishes?

- ► Both x and y are still 0.
- ► x is now 1, but y is still 0.
- **► x is still 0, but y is now 2.**
- ► x is now 1, and y is now 2.

Question No: 6 (Marks: 1) - Please choose one

The difference between a binary tree and a binary search tree is that ,

- **► a binary search tree has two children per node whereas a binary tree can have none, one, or two children per node** Click here for detail
- ► in binary search tree nodes are inserted based on the values they contain
- ► in binary tree nodes are inserted based on the values they contain
- ► none of these

Question No: 7 (Marks: 1) - Please choose one

Compiler uses which one of the following to evaluate a mathematical equation,

- ► Binary Tree
- ► Binary Search Tree
- **► Parse Tree (Page 274)**
- ► AVL Tree

Question No: 8 (Marks: 1) - Please choose one

If there are 56 internal nodes in a binary tree then how many external nodes this binary tree will have?

- ► 54
- ► 55
- ► 56
- **► 57 (Page 303)**

Question No: 9 (Marks: 1) - Please choose one

If there are 23 external nodes in a binary tree then what will be the no. of internal nodes in this binary tree?

- ► 23
- ► 24
- ► 21
- **► 22 (n-1) (Page 304)**

Question No: 10 (Marks: 1) - Please choose one

Which of the following method is helpful in creating the heap at once?

- ► insert
- ► add
- ► update
- **► preculateDown (Page 358)**

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Question No: 11 (Marks: 1) - Please choose one
The definition of Transitivity property is

- ► For all element x member of S, x R x
- ► For all elements x and y, x R y if and only if y R x
- ► **For all elements x, y and z, if x R y and y R z then x R z (Page 385)**
- ► For all elements w, x, y and z, if x R y and w R z then x R z

Question No: 12 (Marks: 1) - Please choose one
A binary tree of N nodes has _____.

- ► Log_{10} N levels
- ► **Log_2 N levels (Page 349)**
- ► N / 2 levels
- ► N x 2 levels

Question No: 13 (Marks: 1) - Please choose one
If there are N elements in an array then the number of maximum steps needed to find an element using Binary Search is _____ .

- ► N
- ► N^2
- ► $Nlog_2N$
- ► **log_2N (page 440)**

Question No: 14 (Marks: 1) - Please choose one
Consider te following array
23 15 5 12 40 10 7
After the first pass of a particular algorithm, the array looks like
15 12 23 10 7 40
Name the algorithm used

- ► Heap sort
- ► Selection sort
- ► Insertion sort
- ► **Bubble sort**

Question No: 15 (Marks: 1) - Please choose one
If both pointers of the node in a binary tree are NULL then it will be a/an _____ .

- ► Inner node
- ► **Leaf node (Page 313)**
- ► Root node
- ► None of the given options

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Question No: 16 (Marks: 1) - Please choose one
By using _____we avoid the recursive method of traversing a Tree, which makes use of stacks and consumes a lot of memory and time.

- ► Binary tree only
- ► **Threaded binary tree (page 306)**
- ► Heap data structure
- ► Huffman encoding

Question No: 17 (Marks: 1) - Please choose one
A complete binary tree of height *3* has between _____ nodes.

- ► 8 to 14
- ► **8 to 15 (Page 124)**
- ► 8 to 16
- ► 8 to 17

2^(d+1) - 1 = 2^(3+1) -1 = 2^4 -1 = 16-1 = 15

Question No: 18 (Marks: 1) - Please choose one
Consider a min heap, represented by the following array:
3,4,6,7,5,10
After inserting a node with value 1.Which of the following is the updated min heap?

- ► 3,4,6,7,5,10,1
- ► 3,4,6,7,5,1,10
- ► 3,4,1,5,7,10,6
- ► **1,4,3,5,7,10,6 close to correct but correct ans is 1,4,3,7,5,10,6 (page 337)**

Question No: 19 (Marks: 1) - Please choose one
Consider a min heap, represented by the following array:
10,30,20,70,40,50,80,60
After inserting a node with value 31.Which of the following is the updated min heap?

- ► **10,30,20,31,40,50,80,60,70 (page 337)**
- ► 10,30,20,70,40,50,80,60,31
- ► 10,31,20,30,40,50,80,60,31
- ► 31,10,30,20,70,40,50,80,60

Question No: 20 (Marks: 1) - Please choose one
Which one of the following algorithms is most widely used due to its good average time,

- ► Bubble Sort
- ► Insertion Sort
- ► **Quick Sort Click here for detail**
- ► Merge Sort

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Question No: 21 (Marks: 1) - Please choose one
Which of the following statement is correct about find(x) operation:

► A find(x) on element x is performed by returning exactly the same node that is found.
► **A find(x) on element x is performed by returning the root of the tree containing x**.
Click here for detail
► A find(x) on element x is performed by returning the whole tree itself containing x. (Page 10)
► A find(x) on element x is performed by returning TRUE.

Question No: 22 (Marks: 1) - Please choose one
Which of the following statement is NOT correct about find operation:

► It is not a requirement that a find operation returns any specific name, just that finds on two elements return the same answer if and only if they are in the same set.
► **One idea might be to use a tree to represent each set, since each element in a tree has the same root, thus the root can be used to name the set.**
► Initially each set contains one element.
► Initially each set contains one element and it does not make sense to make a tree of one node only.

Question No: 23 (Marks: 1) - Please choose one
The following are statements related to queues.
The last item to be added to a queue is the first item to be removed False statement
A queue is a structure in which both ends are not used False statement
The last element hasn't to wait until all elements preceding it on the queue are removed False statement
queue is said to be a last-in-first-out list or LIFO data structure. False statement

Which of the above is/are related to normal queues?
► (iii) and (ii) only
► (i), (ii) and (iv) only
► (ii) and (iv) only
► **None of the given options**

Question No: 24 (Marks: 1) - Please choose one
The maximum number of external nodes (leaves) for a binary tree of height H is _____
► 2^H **Click here for detail**
► 2^H+1
► 2^H-1
► 2^H+2

Question No: 25 (Marks: 1) - Please choose one
In complete binary tree the bottom level is filled from _____
► **Left to right (Page 323)**
► Right to left
► Not filled at all
► None of the given options

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Question No: 26 (Marks: 1) - Please choose one
We are given N items to build a heap, this can be done with _____ successive inserts.

► N-1
► **N (Page 353)**
► N+1
► N^2

Question No: 27 (Marks: 1) - Please choose one
Suppose we had a hash table whose hash function is "n % 12", if the number 35 is already in the hash table, which of the following numbers would cause a collision?

► 144
► 145
► **143**
► 148

Question No: 28 (Marks: 1) - Please choose one
Here is an array of ten integers:
5 3 8 9 1 7 0 2 6 4
The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest to largest).

► **0 3 8 9 1 7 5 2 6 4 (Page 477)**
► 2 6 4 0 3 8 9 1 7 5
► 2 6 4 9 1 7 0 3 8 5
► 0 3 8 2 6 4 9 1 7 5

Question No: 29 (Marks: 1) - Please choose one
What requirement is placed on an array, so that *binary search* may be used to locate an entry?

► The array elements must form a heap.
► The array must have at least 2 entries.
► **The array must be sorted. Click here for detail**
► The array's size must be a power of two.

Question No: 30 (Marks: 1) - Please choose one
In case of deleting a node from AVL tree, rotation could be prolong to the *root* node.

► **Yes (Page 267)**
► No

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FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
_____ only removes items in reverse order as they were entered.

► **Stack (Page 81)**
► Queue
► Both of these
► None of these

Question No: 2 (Marks: 1) - Please choose one
Here is a small function definition:

```
void f(int i, int &k)
{
i = 1;
k = 2;
}
```

Suppose that a main program has two integer variables x and y, which are given the value 0. Then the main program calls f(x,y); What are the values of x and y after the function f finishes?

► Both x and y are still 0.
► x is now 1, but y is still 0.
► **x is still 0, but y is now 2.**
► x is now 1, and y is now 2.

Question No: 3 (Marks: 1) - Please choose one
Select the one *FALSE* statement about binary trees:

► **Every binary tree has at least one node. (Page 113)**
► Every non-empty tree has exactly one root node.
► Every node has at most two children.
► Every non-root node has exactly one parent.

Question No: 4 (Marks: 1) - Please choose one
Every AVL is _____

► Binary Tree
► Complete Binary Tree
► None of these
► **Binary Search Tree** **Click here for detail**

Question No: 5 (Marks: 1) - Please choose one
Searching an element in an AVL tree take maximum _____ time (where n is no. of nodes in AVL tree),

► $Log_2(n+1)$
► $Log_2(n+1) -1$
► **$1.44\ Log_2 n$ (Page 227)**
► $1.66\ Log_2 n$

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Question No: 6 (Marks: 1) - Please choose one
Suppose that we have implemented a *priority queue* by storing the items in a heap. We are now executing a reheapification downward and the out-of-place node has priority of 42. The node's parent has a priority of 72, the left child has priority 52 and the node's right child has priority 62. Which statement best describes the status of the reheapification.

- ► The reheapification is done.
- ► The next step will interchange the two children of the out-of-place node.
- ► The next step will swap the out-of-place node with its parent.
- ► The next step will swap the out-of-place node with its left child.

Question No: 7 (Marks: 1) - Please choose one
Suppose you implement a heap (with the largest element on top) in an array. Consider the different arrays below, determine the one that *cannot* possibly be a heap:

- ► 7 6 5 4 3 2 1
- ► 7 3 6 2 1 4 5
- ► 7 6 4 3 5 2 1
- ► **7 3 6 4 2 5 1**

According to max heap property

Question No: 8 (Marks: 1) - Please choose one
If there are 23 external nodes in a binary tree then what will be the no. of internal nodes in this binary tree?

- ► 23
- ► 24
- ► 21
- ► ***22 (N-1)***

Question No: 9 (Marks: 1) - Please choose one
If there are N external nodes in a binary tree then what will be the no. of internal nodes in this binary tree?

- ► **N -1 (Page 304)**
- ► N+1
- ► N+2
- ► N

Question No: 10 (Marks: 1) - Please choose one
Which one of the following is NOT the property of equivalence relation:

- ► Reflexive
- ► Symmetric
- ► Transitive
- ► **Associative (Page 385)**

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Question No: 11 (Marks: 1) - Please choose one
The definition of Transitivity property is
- ► For all element x member of S, x R x
- ► For all elements x and y, x R y if and only if y R x
- ► **For all elements x, y and z, if x R y and y R z then x R z (Page 385)**
- ► For all elements w, x, y and z, if x R y and w R z then x R z

Question No: 12 (Marks: 1) - Please choose one
Union is a _____ time operation.
- ► **Constant (Page 120)**
- ► Polynomial
- ► Exponential
- ► None of the given option

Question No: 13 (Marks: 1) - Please choose one
Which of the following is NOT a correct statement about Table ADT.
► In a table, the type of information in columns may be different. yes
► **A table consists of several columns, known as entities. (Page 408)**
► The row of a table is called a record.
► A major use of table is in databases where we build and use tables for keeping information.

Question No: 14 (Marks: 1) - Please choose one
In the worst case of deletion in AVL tree requires _____.
- ► Only one rotation
- ► Rotation at each non-leaf node
- ► Rotation at each leaf node
- ► **Rotations equal to log2 N (Page 441)**

Question No: 15 (Marks: 1) - Please choose on
Binary Search is an algorithm of searching, used with the _____ data.
► **Sorted (Page 432)**
► Unsorted
► Heterogeneous
► Random

Question No: 16 (Marks: 1) - Please choose on
Which of the following statement is correct?
► A Threaded Binary Tree is a binary tree in which every node that does not have a left child has a THREAD (in actual sense, a link) to its INORDER successor.
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its PREOREDR successor.
► **A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its INORDER successor. (Page 307)**
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its POSTORDER successor.

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Question No: 17 (Marks: 1) - Please choose one

By using _____we avoid the recursive method of traversing a Tree, which makes use of stacks and consumes a lot of memory and time.

- ► Binary tree only
- ► **Threaded binary tree (page 306)**
- ► Heap data structure
- ► Huffman encoding

Question No: 18 (Marks: 1) - Please choose one

Which of the following statement is NOT true about threaded binary tree?

- ► Right thread of the right-most node points to the *dummy* node.
- ► Left thread of the left-most node points to the *dummy* node.
- ► The left pointer of dummy node points to the root node of the tree.
- ► **Left thread of the right-most node points to the *dummy* node. (page 321)**

Question No: 19 (Marks: 1) - Please choose one

Consider a min heap, represented by the following array:
11,22,33,44,55
After inserting a node with value 66.Which of the following is the updated min heap?

- ► **11,22,33,44,55,66 (page 337)**
- ► 11,22,33,44,66,55
- ► 11,22,33,66,44,55
- ► 11,22,66,33,44,55

Question No: 20 (Marks: 1) - Please choose one

Consider a min heap, represented by the following array:
3,4,6,7,5
After calling the function deleteMin().Which of the following is the updated min heap?

- ► 4,6,7,5
- ► 6,7,5,4
- ► **4,5,6,7 (page 349)**
- ► 4,6,5,7

Question No: 21 (Marks: 1) - Please choose one

We can build a heap in _____ time.

- ► **Linear (Page 353)**
- ► Exponential
- ► Polynomial
- ► None of the given options

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Question No: 22 (Marks: 1) - Please choose one

Suppose we are sorting an array of eight integers using quick sort, and we have just finished the first partitioning with the array looking like this:

2 5 1 7 9 12 11 10

Which statement is correct?

- **► The pivot could be either the 7 or the 9. (page 506)**
- ► The pivot could be the 7, but it is not the 9.
- ► The pivot is not the 7, but it could be the 9
- ► Neither the 7 nor the 9 is the pivot.

Question No: 23 (Marks: 1) - Please choose one

Which formula is the best approximation for the depth of a heap with n nodes?

- **► log (base 2) of n (Page 353)**
- ► The number of digits in n (base 10), e.g., 145 has three digits
- ► The square root of n
- ► n

Question No: 24 (Marks: 1) - Please choose one

Suppose you implement a Min heap (with the smallest element on top) in an array. Consider the different arrays below; determine the one that *cannot* possibly be a heap:

- ► 16, 18, 20, 22, 24, 28, 30
- ► 16, 20, 18, 24, 22, 30, 28
- ► 16, 24, 18, 28, 30, 20, 22
- **► 16, 24, 20, 30, 28, 18, 22 It's not satisfy the min heap property.**

Question No: 25 (Marks: 1) - Please choose one

While joining nodes in the building of Huffman encoding tree if there are more nodes with same frequency, we choose the nodes _____.

- **► Randomly (Page 289)**
- ► That occur first in the text message
- ► That are lexically smaller among others.
- ► That are lexically greater among others

Question No: 26 (Marks: 1) - Please choose one

Consider the following paragraph with blanks.

A …….. is a linear list where …… and …… take place at the same end . This end is called the ……

What would be the correct filling the above blank positions?

- ► (i) queue (ii) insertion (iii) removals (iv) top
- ► (i) stack (ii) insertion (iii) removals (iv) bottom
- **► (i) stack (ii) insertion (iii) removals (iv) top (Page 52)**
- ► (i) tree (ii) insertion (iii) removals (iv) top

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Question No: 27 (Marks: 1) - Please choose one
A binary tree with 33 internal nodes has _____ links to internal nodes.

- ► 31
- ► **32 (n-1 links to internal nodes) (Page 304)**
- ► 33
- ► 66 .

Question No: 28 (Marks: 1) - Please choose on
Which traversal gives a decreasing order of elements in a heap where the max element is stored at the top?

- ► post-order
- ► level-order
- ► inorder
- ► **None of the given options**

Question No: 29 (Marks: 1) - Please choose one
What requirement is placed on an array, so that *binary search* may be used to locate an entry

- ► The array elements must form a heap.
- ► The array must have at least 2 entries.
- ► **The array must be sorted** **Click here for detail**
- ► The array's size must be a power of two.

Question No: 30 (Marks: 1) - Please choose one
Which of the following is a non linear data structure?

- ► Linked List
- ► Stack
- ► Queue
- ► **Tree (Page 112)**

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The data of the problem is of 2GB and the hard disk is of 1GB capacity, to solve this problem we should

- ► Use better data structures
- ► **Increase the hard disk space (Page 5)**
- ► Use the better algorithm
- ► Use as much data as we can store on the hard disk

Question No: 2 (Marks: 1) - Please choose one
In an array list the current element is

- ► **The first element** **Click here for detail**

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► The middle element
► The last element
► The element where the current pointer points to

Question No: 3 (Marks: 1) - Please choose one
Which one of the following is a valid postfix expression?

► ab+c*d-
► **abc*+d- (According to rule)**
► abc+*d-
► (abc*)+d-

Question No: 4 (Marks: 1) - Please choose one
In sequential access data structure, accessing any element in the data structure takes different amount of time. Tell which one of the following is sequential access data structure,

► Arrays
► **Lists** **Click here for detail**
► Both of these
► None of these

Question No: 5 (Marks: 1) - Please choose one
I have implemented the queue with a circular array. If data is a circular array of CAPACITY elements, and last is an index into that array, what is the formula for the index after last?
► (last % 1) + CAPACITY
► last % (1 + CAPACITY)
► **(last + 1) % CAPACITY**
► last + (1 % CAPACITY)
This expression will point to field after last that will be the first field.

Question No: 6 (Marks: 1) - Please choose one
Which one of the following is TRUE about recursion?

► **Recursion extensively uses stack memory. (page 149)**
► Threaded Binary Trees use the concept of recursion.
► Recursive function calls consume a lot of memory.
► Iteration is more efficient than iteration.

Question No: 7 (Marks: 1) - Please choose one
Compiler uses which one of the following to evaluate a mathematical equation,

► Binary Tree
► Binary Search Tree
► **Parse Tree (Page 274)**
► AVL Tree

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Question No: 8 (Marks: 1) - Please choose one
Which one of the following is TRUE about iteration?

- ► Iteration extensively uses stack memory.
- ► Threaded Binary Trees use the concept of iteration.
- ► Iterative function calls consumes a lot of memory.
- ► **Recursion is more efficient than iteration.** **Click here for detail**

Question No: 9 (Marks: 1) - Please choose one
If a max heap is implemented using a partially filled array called data, and the array contains n elements (n > 0), where is the entry with the greatest value? **Data[0] is correct**

- ► data[1]
- ► data[n-1]
- ► data[n]
- ► data[2*n+1]

Question No: 10 (Marks: 1) - Please choose one
If there are 56 internal nodes in a binary tree then how many external nodes this binary tree will have?

- ► 54
- ► 55
- ► 56
- ► **57 (n+1)**

Question No: 11 (Marks: 1) - Please choose one
Which of the following heap method increase the value of key at position 'p' by the amount 'delta'?

- ► **increaseKey(p,delta) (Page 363)**
- ► decreaseKey(p,delta)
- ► preculateDown(p,delta)
- ► remove(p,delta)

Question No: 12 (Marks: 1) - Please choose one
If we have 1000 sets each containing a single different person. Which of the following relation will be true on each set:

- ► **Reflexive (page 387)**
- ► Symmetric
- ► Transitive
- ► Associative

Question No: 13 (Marks: 1) - Please choose one
Which one of the following is not an example of equivalence relation:

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► Electrical connectivity
► Set of people
► **<= relation (Page 388)**
► Set of pixels

Question No: 14 (Marks: 1) - Please choose one
A binary tree of N nodes has _____.

► Log_{10} N levels
► **Log_2 N levels (Page 212)**
► N / 2 levels
► N x 2 levels

Question No: 15 (Marks: 1) http://vustudents.ning.com - Please choose one
Binary Search is an algorithm of searching, used with the _____ data.
► **Sorted (Page 432)**
► Unsorted
► Heterogeneous
► Random

Question No: 16 (Marks: 1) - Please choose one
Consider te following array
23 15 5 12 40 10 7
After the first pass of a particular algorithm, the array looks like
15 5 12 23 10 7 40
Name the algorithm used

► Heap sort
► Selection sort
► Insertion sort
► **Bubble sort (According to rule)**

Question No: 17 (Marks: 1) - Please choose one
Which of the following statements is correct property of binary trees?
► A binary tree with N internal nodes has N+1 internal links.
► A binary tree with N external nodes has 2N internal nodes.
► **A binary tree with N internal nodes has N+1 external nodes. (page 304)**
► None of above statement is a property of the binary tree.

Question No: 18 (Marks: 1) - Please choose one
Which of the following is a property of binary tree?
► A binary tree of N external nodes has N internal node.
► **A binary tree of N internal nodes has N+ 1 external node. (Page 304)**
► A binary tree of N external nodes has N+ 1 internal node.
► A binary tree of N internal nodes has N- 1 external node.

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Question No: 19 (Marks: 1) - Please choose one
Which of the following statement is true about dummy node of threaded binary tree?

► The left pointer of dummy node points to the itself while the right pointer points to the root of tree.

► **The left pointer of dummy node points to the root node of the tree while the right pointer points itself i.e. to *dummy* node (Page 321)**

► The left pointer of dummy node points to the root node of the tree while the right pointer is always NULL.

► The right pointer of dummy node points to the itself while the left pointer is always NULL.

Question No: 20 (Marks: 1) - Please choose one
If the bottom level of a binary tree is NOT completely filled, depicts that the tree is NOT a

► Expression tree
► Threaded binary tree
► **complete Binary tree (Page 323)**
► Perfectly complete Binary tree

Question No: 21 (Marks: 1) - Please choose one
In a selection sort of n elements, how many times the swap function is called to complete the execution of the algorithm?

► **n-1** **Click here for detail**
► n log n
► n^2
► 1

Question No: 22 (Marks: 1) - Please choose one
Which of the following statement is correct about find(x) operation:

► A find(x) on element x is performed by returning exactly the same node that is found.

►**A find(x) on element x is performed by returning the root of the tree containing x.** Click here for detail

► A find(x) on element x is performed by returning the whole tree itself containing x.

► A find(x) on element x is performed by returning TRUE.

Question No: 23 (Marks: 1) - Please choose one
Which of the following statement is NOT correct about find operation:

► It is not a requirement that a find operation returns any specific name, just that finds on two elements return the same answer if and only if they are in the same set.

► **One idea might be to use a tree to represent each set, since each element in a tree has the same root, thus the root can be used to name the set.**

► Initially each set contains one element.

► **Initially** each set contains one element and it does not make sense to make a tree of one node only.

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Question No: 24 (Marks: 1) - Please choose one
Consider the following postfix expression S and the initial values of the variables.

S = A B - C + D E F - + ^
Assume that A=3, B=2, C=1, D=1, E=2, F=3

What would be the final output of the stack?

► **1** **Click here for detail**
► 2
► 0
► -1

Question No: 25 (Marks: 1) - Please choose one
The maximum number of external nodes (leaves) for a binary tree of height H is _____
► **2^H** **Click here for detail**
► 2^H+1
► 2^H-1
► 2^H+2

Question No: 26 (Marks: 1) - Please choose one
In threaded binary tree the NULL pointers are replaced by ,

► preorder successor or predecessor
► **inorder successor or predecessor (Page 307)**
► postorder successor or predecessor
► NULL pointers are not replaced

Question No: 27 (Marks: 1) - Please choose one
In a min heap , preculateDown procedure will move smaller value_____ and bigger value_____.
► left,right
► right,left
► **up,down (Page 358)**
► down,up

Question No: 28 (Marks: 1) - Please choose one
Which of the following statement is correct about union:
► **To perform Union of two sets, we merge the two trees by making the root of one tree point to the root of the other. (Greedy algorithms , Page 7)**
► To perform Union of two sets, we merge the two trees by making the leaf node of one tree point to the root of the other.
► To perform Union of two sets, merging operation of trees in not required at all.
► None of the given options.

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Question No: 29 (Marks: 1) - Please choose one
Suppose A is an array containing numbers in increasing order, but some numbers occur more than once when using a binary search for a value, the binary search always finds _____

- ► **the first occurrence of a value.** **Click here for detail**
- ► the second occurrence of a value.
- ► may find first or second occurrence of a value.
- ► None of the given options.

Question No: 30 (Marks: 1) - Please choose one
Let heap stored in an array as H = [50, 40, 37, 32, 28, 22, 36, 13]. In other words, the root of the heap contains the maximum element. What is the result of deleting 40 from this heap

- ► **[50,32, 37,13, 28, 22, 36] according to max heap property.**
- ► [37, 28, 32, 22, 36, 13]
- ► [37, 36, 32, 28, 13, 22]
- ► [37, 32, 36, 13, 28, 22]

FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
In an array we can store data elements of different types.

- ► True
- ► **False**

Question No: 2 (Marks: 1) - Please choose one
Which one of the following statement is NOT correct .

- ► In linked list the elements are necessarily to be contiguous
- ► **In linked list the elements may locate at far positions in the memory (page 18)**
- ► In linked list each element also has the address of the element next to it
- ► In an array the elements are contiguous

Question No: 3 (Marks: 1) - Please choose one
Doubly Linked List always has one NULL pointer.

- ► True
- ► **False(page 39)**

Question No: 4 (Marks: 1) - Please choose one

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A queue is a data structure where elements are,

- ► **inserted at the front and removed from the back. .(see example at page #89 nd 90)**
- ► inserted and removed from the top.
- ► inserted at the back and removed from the front.
- ► inserted and removed from both ends.

Question No: 5 (Marks: 1) - Please choose one
Each node in doubly link list has,

- ► 1 pointer
- ► **2 pointers(page 39)**
- ► 3 pointers
- ► 4 pointers

Question No: 6 (Marks: 1) - Please choose one
I have implemented the queue with a linked list, keeping track of a front pointer and a rear pointer. Which of these pointers will change during an insertion into an *EMPTY* queue?

- ► Neither changes
- ► Only front pointer changes.
- ► Only rear pointer changes.
- ► **Both change.**

Since it is an empty queue the front and rear are initialize to -1, so on insertion both the pointers will change and point to 0.

Question No: 7 (Marks: 1) - Please choose one
Compiler uses which one of the following to evaluate a mathematical equation,

- ► Binary Tree
- ► Binary Search Tree
- ► **Parse Tree(page 274)**
- ► AVL Tree

Question No: 8 (Marks: 1) - Please choose one
If a complete binary tree has n number of nodes then its height will be,

- ► **$Log_2 (n+1) -1$(page 139)**
- ► 2^n
- ► $Log_2 (n) - 1$
- ► $2^n - 1$

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Question No: 9 (Marks: 1) - Please choose one
If a complete binary tree has height h then its no. of nodes will be,

- ► Log (h)
- ► **2^{h+1}- 1(page 324)**
- ► Log (h) - 1
- ► 2^h - 1

Question No: 10 (Marks: 1) http://vustudents.ning.com - Please choose one
A binary relation R over S is called an equivalence relation if it has following property(s)

- ► Reflexivity
- ► Symmetry
- ► Transitivity
- ► **All of the given options (page 387)**

Question No: 11 (Marks: 1) - Please choose one
Binary Search is an algorithm of searching, used with the _____ data.

- ► **Sorted (page 432)**
- ► Unsorted
- ► Heterogeneous
- ► Random

Question No: 12 (Marks: 1) - Please choose one
If there are N elements in an array then the number of maximum steps needed to find an element using Binary Search is _____ .

- ► N
- ► N^2
- ► $N\log_2 N$
- ► **$\log_2 N$ (page 440)**

Question No: 13 (Marks: 1) - Please choose one
Use of binary tree in compression of data is known as _____ .

- ► Traversal
- ► Heap
- ► Union
- ► **Huffman encoding (page 287)**

Question No: 14 (Marks: 1) - Please choose one
While building Huffman encoding tree the new node that is the result of joining two nodes has the frequency.

- ► Equal to the small frequency
- ► Equal to the greater
- ► **Equal to the sum of the two frequencies (page 293)**
- ► Equal to the difference of the two frequencies

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Question No: 15 (Marks: 1) - Please choose one
Which of the following statements is correct property of binary trees?

► A binary tree with N internal nodes has N+1 internal links.
► A binary tree with N external nodes has 2N internal nodes.
► **A binary tree with N internal nodes has N+ 1 external node. (page 303)**
► None of above statement is a property of the binary tree.

Question No: 16 (Marks: 1) - Please choose one
Which of the following is a property of binary tree?

► A binary tree of N external nodes has N internal node.
► **A binary tree of N internal nodes has N+ 1 external node. (page 303)**
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► A binary tree of N internal nodes has N- 1 external node.

Question No: 17 (Marks: 1) - Please choose one
Which of the following statement is correct?

► A Threaded Binary Tree is a binary tree in which every node that does not have a left child has a THREAD (in actual sense, a link) to its INORDER successor.
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its PREOREDR successor.
► **A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its INORDER successor. (Page 307)**
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its POSTORDER successor.

Question No: 18 (Marks: 1) - Please choose one
Which of the following statement is correct?

► A Threaded Binary Tree is a binary tree in which every node that does not have a left child has a THREAD (in actual sense, a link) to its INORDER successor.
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its PREOREDR successor.
► **A Threaded Binary Tree is a binary tree in which every node that does not have a left child has a THREAD (in actual sense, a link) to its INORDER predecessor.**
► A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its POSTORDER predecessor.

Question No: 19 (Marks: 1) - Please choose one
A Threaded Binary Tree is a binary tree in which every node that does not have a right child has a THREAD (in actual sense, a link) to its _____ successor.

► levelorder
► Preorder

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► **Inorder** **Click here for detail**
► Postorder

Question No: 20 (Marks: 1) - Please choose one
Which of the following statement is true about dummy node of threaded binary tree?
► This dummy node never has a value.
► This dummy node has always some dummy value.
► **This dummy node has either no value or some dummy value. .(page 321)**
► This dummy node has always some integer value.

Question No: 21 (Marks: 1) - Please choose one
A complete binary tree is a tree that is _____ filled, with the possible exception of the bottom level.
► partially
► **completely (page 323)**
► incompletely
► partly

Question No: 22 (Marks: 1) - Please choose one
A complete binary tree of height *3* has between _____ nodes.
► 8 to 14
► **8 to 15 (page 124)**
► 8 to 16
► 8 to 17

Question No: 23 (Marks: 1) - Please choose one
We can build a heap in _____ time.

► **Linear (page 353)**
► Exponential
► Polynomial
► None of the given options

Question No: 24 (Marks: 1) - Please choose one
Suppose that a selection sort of 100 items has completed 42 iterations of the main loop. How many items are now guaranteed to be in their final spot (never to be moved again)?

► 21
► 41
► **42** **Click here for detail**
► 43

Question No: 25 (Marks: 1) - Please choose one
Suppose you implement a Min heap (with the smallest element on top) in an array. Consider the different arrays below; determine the one that *cannot* possibly be a heap:
► 16, 18, 20, 22, 24, 28, 30

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► 16, 20, 18, 24, 22, 30, 28
► 16, 24, 18, 28, 30, 20, 22
► **16, 24, 20, 30, 28, 18, 22** **It's not satisfy the min heap property**

Question No: 26 (Marks: 1) - Please choose one
Which of the following statement is NOT correct about find operation:

► It is not a requirement that a find operation returns any specific name, just that finds on two elements return the same answer if and only if they are in the same set.
► **One idea might be to use a tree to represent each set, since each element in a tree has the same root, thus the root can be used to name the set.**
► Initially each set contains one element.
► Initially each set contains one element and it does not make sense to make a tree of one node only.

Question No: 27 (Marks: 1) - Please choose one
Consider the following infix expression:
x – y * a + b / c
Which of the following is a correct equivalent expression(s) for the above?

► x y -a * b +c /
► x *y a - b c / +
► **x y a * - b c / +** **Hint :- (x – y * a) +(b / c)**
► x y a * - b/ + c

Question No: 28 (Marks: 1) - Please choose one
A complete binary tree of height ____ has nodes between 16 to 31 .
► 2
► 3
► **4 (page 124)**
► 5

Question No: 29 (Marks: 1) - Please choose one
Here is an array of ten integers:
5 3 8 9 1 7 0 2 6 4
The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest to largest).

► **0 3 8 9 1 7 5 2 6 4 (Page 477)**
► 2 6 4 0 3 8 9 1 7 5
► 2 6 4 9 1 7 0 3 8 5
► 0 3 8 2 6 4 9 1 7 5

Question No: 30 (Marks: 1) - Please choose one
What requirement is placed on an array, so that *binary search* may be used to locate an entry?

► The array elements must form a heap.

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- The array must have at least 2 entries.
- **The array must be sorted.** **Click here for detail**
- The array's size must be a power of two.

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FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356)**

Question No: 2 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► **Current state and external input (Page 318)**
- ► Input and clock signal applied

Question No: 3 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 299)**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 4 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221)**
- ► False

Question No: 5 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 6 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 7 (Marks: 1) - Please choose one
_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 8 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369)**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 9 (Marks: 1) - Please choose one
A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter
- ► **Mod-10 counter (Page 274)**

Question No: 10 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

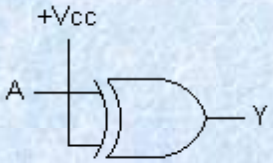
- ► It is set to logic low
- ► **It is set to logic high (Page 356)**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

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Question No: 11 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Question No: 12 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here for detail**
- ► $\overline{A}$

Question No: 13 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- ► 1110
- ► 1100
- ► 1000
- ► **0000 (Page 34)**

Question No: 14 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **Vout / Vin = - Rf / Ri (Page 446)**
- ► Vout / Rf = - Vin / Ri
- ► Rf / Vin = - Ri / Vout
- ► Rf / Vin = Ri / Vout

Question No: 15 (Marks: 1) - Please choose one
LUT is acronym for _____

- ► **Look Up Table (Page 439)**
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

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Question No: 16 (Marks: 1) - Please choose one
The three fundamental gates are _____

- ► AND, NAND, XOR
- ► OR, AND, NAND
- ► NOT, NOR, XOR
- ► **NOT, OR, AND (Page 40)**

Question No: 17 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- ► The organization of memory
- ► The structure of memory
- ► The size of decoding unit
- ► **The size of the address bus of the microprocessor (Page 430)**

Question No: 18 (Marks: 1) - Please choose one
Stack is an acronym for _____

- ► FIFO memory
- ► **LIFO memory (Page 429)**
- ► Flash Memory
- ► Bust Flash Memory

Question No: 19 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

- ► 213
- ► 123
- ► **127**
- ► 345

Question No: 20 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 21 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- ► Race condition
- ► **Clock Skew (Page 226)**
- ► Ripple Effect
- ► None of given options

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Question No: 22 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

- ► 0000
- ► **1101 (not sure)**
- ► 1011
- ► 1111

Question No: 23 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- ► **Current state and the inputs (Page 332)**
- ► Current state and outputs
- ► Previous state and inputs
- ► Previous state and outputs

Question No: 24 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335)**

Question No: 25 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

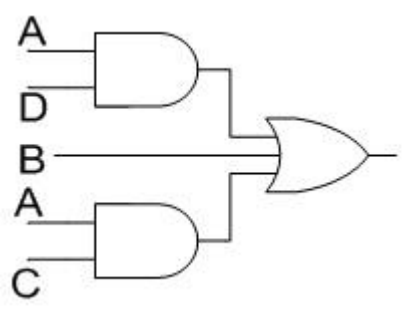
- ► 1100
- ► 0011
- ► **0000** Click here for detail
- ► 1111

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Question No: 27 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

. **Question No: 28 (Marks: 1) - Please choose one**
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

Question No: 29 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 30 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 31 (Marks: 1) - Please choose one
A GAL is essentially a _____.

► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

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Question No: 32 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► **FAST Mode Page Access (Page 413)**
- ► None of given options

Question No: 33 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 34 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 2 (Marks: 1) - Please choose one
A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301)**
- ► Counts high and low range of given clock pulse
- ► None of given options

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Question No: 3 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► Current state and external input
- ► **Input and clock signal applied (Page 305)**

Question No: 4 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 229) rep**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221) rep**
- ► False

Question No: 6 (Marks: 1) - Please choose one
Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228)**
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242) rep**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

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Question No: 9 (Marks: 1) - Please choose one

_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 10 (Marks: 1) - Please choose one

Given the state diagram of an up/down counter, we can find _____

- ► **The next state of a given present state (Page 371)**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

- ► two AND gates, two OR gates, two inverters
- ► three AND gates, two OR gates, one inverter
- ► **two AND gates, one OR gate, two inverters (Lecture 8)**
- ► two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter
- ► **Mod-10 counter (Page 274)**

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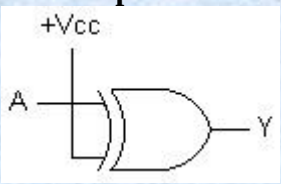
Question No: 14 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 15 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here for detail** **rep**
- ► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- ► 1110
- ► 1100
- ► 1000
- ► **0000 (Page 34) rep**

Question No: 18 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

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Question No: 19 (Marks: 1) - Please choose one
LUT is acronym for _____

- **Look Up Table (Page 439) rep**
- Local User Terminal
- Least Upper Time Period
- None of given options

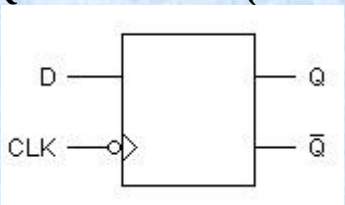
Question No: 20 (Marks: 1) - Please choose one
DRAM stands for _____

- **Dynamic RAM (Page 407)**
- Data RAM
- Demoduler RAM
- None of given options

Question No: 21 (Marks: 1) - Please choose one
The three fundamental gates are _____

- AND, NAND, XOR
- OR, AND, NAND
- NOT, NOR, XOR
- **NOT, OR, AND (Page 40)**

Question No: 22 (Marks: 1) - Please choose one



Which of the following statement is true regarding above block diagram?

- Triggering takes place on the negative-going edge of the CLK pulse
- Triggering takes place on the positive-going edge of the CLK pulse
- Triggering can take place anytime during the HIGH level of the CLK waveform
- Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- The organization of memory
- The structure of memory
- The size of decoding unit
- **The size of the address bus of the microprocessor (Page 430) rep**

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Question No: 24 (Marks: 1) - Please choose one
The expression F=A+B+C describes the operation of three bits _____ Gate.

► **OR (Page 42)**
► AND
► NOT
► NAND

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for_____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

► 213
► 123
► **127**
► 345

FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

► 8-bit
► 16-bit
► **32-bit (Page 25)**
► 64-bit

Question No: 2 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____

► 11101
► 11011
► **10111 (According to rule)**
► 11110

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Question No: 3 (Marks: 1) - Please choose one
The basic building block for a logical circuit is _____

- ► A Flip-Flop
- ► **A Logical Gate (Page 7)**
- ► An Adder
- ► None of given options

Question No: 4 (Marks: 1) - Please choose one
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

- ► Undefined
- ► One
- ► **Zero (According to rule)**
- ► No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

- ► 2
- ► 8
- ► **12 (According to rule "2^n")**
- ► 16

Question No: 6 (Marks: 1) - Please choose one
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

- ► **AND (Page 182)**
- ► OR
- ► NOT
- ► XOR

Question No: 7 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235) rep**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 8 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

- ► J-K input
- ► S-R input
- ► D input
- ► **Clear Input (CLR) (Page 235)**

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Question No: 9 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

► **Asynchronous, synchronous (Page 369) rep**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 11 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101 (not sure)**
► 1011
► 1111

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

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Question No: 14 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335)**

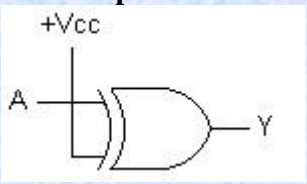
Question No: 15 (Marks: 1) - Please choose one

The best state assignment tends to _____.

- ► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
- ► Minimizes the number of state variables that don't change in a group of related states
- ► Minimize the equivalent states
- ► None of given options

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for detail rep**
- ► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 18 (Marks: 1) - Please choose one

5-bit Johnson counter sequences through ____ states

- ► 7
- ► **10 (Page 354)**
- ► 32
- ► 25

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Question No: 19 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► 1100
- ► 0011
- ► **0000** **Click here for detail rep**
- ► 1111

Question No: 20 (Marks: 1) - Please choose one

The address from which the data is read, is provided by _____

- ► Depends on circuitry
- ► None of given options
- ► RAM
- ► **Microprocessor (Page 397)**

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- ► **First In, First Out (Page 424)**
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one

LUT is acronym for _____

- ► **Look Up Table (Page 439) rep**
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

Question No: 23 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

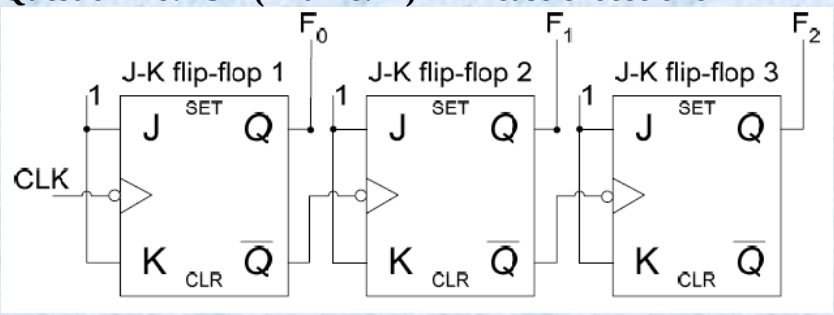
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Question No: 24 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- ► Resolution
- ► **Accuracy (Page 460) rep**
- ► Quantization
- ► Missing Code

Question No: 25 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270)**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 26 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354)**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one

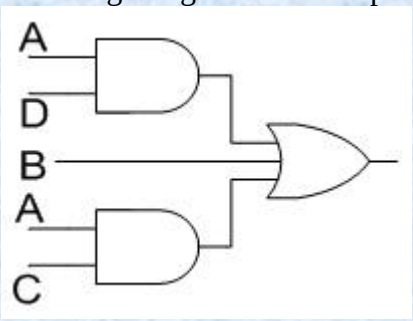
"A + B = B + A" is _____

- ► Demorgan's Law
- ► Distributive Law
- ► **Commutative Law (Page 72)**
- ► Associative Law

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Question No: 2 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► **Sum of product form (Page 78) rep**

Question No: 3 (Marks: 1) - Please choose one

Following is standard POS expression

$$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$$

- ► **True (Lecture 9)**
- ► False

Question No: 4 (Marks: 1) - Please choose one

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

- ► Using a single comparator
- ► **Using Iterative Circuit based Comparators (Page 155)**
- ► Connecting comparators in vertical hierarchy
- ► Extra logic gates are always required.

Question No: 5 (Marks: 1) - Please choose one

Demultiplexer is also called

- ► Data selector
- ► Data router
- ► **Data distributor (Page 178)**
- ► Data encoder

Question No: 6 (Marks: 1) - Please choose one

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

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Question No: 7 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228) rep**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 8 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 9 (Marks: 1) - Please choose one
_____ counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**
► Synchronous
► Positive-Edge triggered
► Negative-Edge triggered

Question No: 10 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

► **ENP, ENT (Page 285) rep**
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 11 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

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Question No: 12 (Marks: 1) - Please choose one
In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

► 3
► **4 (Page 281)**
► 7
► 10

Question No: 14 (Marks: 1) - Please choose one
_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341) rep**
► State reduction
► Next state table
► State diagram

Question No: 15 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 16 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

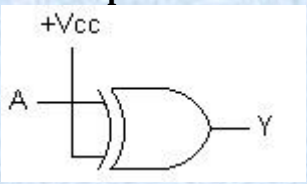
► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 17 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
►**Reprogrammable PAL (Page 183) rep**

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Question No: 18 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here For detail** **rep**
- ► $\overline{A}$

Question No: 20 (Marks: 1) - Please choose one

in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► **FAST Mode Page Access (Page 413) rep**
- ► None of given options

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- ► **First In, First Out (Page 424) rep**
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one

In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425) rep**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 23 (Marks: 1) - Please choose one

A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301) rep**
- ► Counts high and low range of given clock pulse
- ► None of given options

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Question No: 24 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354) rep**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____

- ► FIFO memory
- ► **LIFO memory (Page 429) rep**
- ► Flash Memory
- ► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
The 4-bit 2's complement representation of "+5" is _____

- ► 1010
- ► 1110
- ► 1011
- ► **0101 (Page 22)**

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
The storage cell in SRAM is
- ► a flip –flop
- ► **a capacitor (Page 407)**
- ► a fuse
- ► a magnetic domain

Question No: 2 (Marks: 1) - Please choose one
What is the difference between a D latch and a D flip-flop?
- ► The D latch has a clock input.
- ► The D flip-flop has an enable input.
- ► The D latch is used for faster operation.
- ► **The D flip-flop has a clock input.** **Click here for detail**

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Question No: 3 (Marks: 1) - Please choose one
For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH.
►toggle Click here for detail
►set
►reset
►not change

Question No: 4 (Marks: 1) - Please choose one
The OR gate performs Boolean _____.
►multiplication
►subtraction
►division
►addition (Page 42)

Question No: 5 (Marks: 1) - Please choose one
If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
► set (Page 219)
► reset
► invalid
► clear

5. Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.
►A = 1, B = 0, C = 0, D = 0
►A = 1, B = 0, C = 1, D = 0 (Lecture 8)
►A = 0, B = 1, C = 0, D = 0
►A = 1, B = 0, C = 1, D = 1

Question No: 6 (Marks: 1) - Please choose one
The power dissipation, *P*D, of a logic gate is the product of the
►dc supply voltage and the peak current Click here for detail
►dc supply voltage and the average supply current
►ac supply voltage and the peak current
►ac supply voltage and the average supply current

Question No: 7 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.
►True Click here for detail
►False

Question No: 8 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
►True (Page 50)
►False

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Question No: 9 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
►A parallel to serial converter circuit (Page 244)
►A counter circuit
►A BCD to Decimal decoder
►A 2-to-8 bit decoder

Question No: 10 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
►4
►8 (Page 89)
►12
►16

Question No: 11 (Marks: 1) - Please choose one
In designing any counter the transition from a current state to the next sate is determined by
►Current state and inputs (Page 332)
►Only inputs
►Only current state
►current state and outputs

Question No: 12 (Marks: 1) - Please choose one
Sum term (Max term) is implemented using _____ gates
►OR (Page 78)
►AND
►NOT
►OR-AND

Question No: 13 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► The next state of a given present state (Page 371) rep
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 14 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?
►2
►4
►6
►8 (not sure)

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Question No: 15 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO _____

►THE FLOP-FLOP IS TRIGGERED
►Q=0 AND Q'=1
►Q=1 AND Q'=0 (Page 233)
►THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

Question No: 16 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
►0
►1 (Page 230)
►Invalid
►Input is invalid

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
► 0
► 1
► Invalid (Page 233)
► Input is invalid

Question No: 17 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
►Set-up time
►Hold time (Page 242) rep
►Pulse Interval time
►Pulse Stability time (PST)

Question No: 18 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____
►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
►3
►7
►8 (Page 272)
►15

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Question No: 20 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 21 (Marks: 1) - Please choose one
The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines
►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 22 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
►Ten
►Eight
►Three
►Two (Page 262)

Question No: 23 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
►Race condition
►Clock Skew (Page 226) rep
►Ripple Effect
►None of given options

Question No: 24 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►Parallel in / Serial out shift register (Page 356)
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____
► FIFO memory
► LIFO memory (Page 429) rep
► Flash Memory
► Bust Flash Memory

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Question No: 26 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?
► = 0, Cout = 0
► **= 0, Cout = 1 (Page 135)**
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 27 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____
►GATED FLIP-FLOPS
►PULSE TRIGGERED FLIP-FLOPS
►POSITIVE-EDGE TRIGGERED FLIP-FLOPS
►**NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)**

Question No: 28 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 29 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____
►ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
►MOD-10 AND MOD-6 COUNTERS
►MOD-10 AND MOD-2 COUNTERS
►**A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)**

Question No: 30 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 31 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

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Question No: 32 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

Question No: 33 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

►State diagram
►**Next state table**
►State reduction
►**State assignment (Page 335) rep**

Question No: 34 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

►**1 floating-gate MOS transistor (Page 419)**
►2 floating-gate MOS transistors
►4 floating-gate MOS transistors
►6 floating-gate MOS transistors

Question No: 35 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

►Q2:= Q1 $ X $ Q3
►**Q2:= Q1 # X # Q3 (Page 210)**
►Q2:= Q1 & X & Q3
►Q2:= Q1 ! X ! Q3

Question No: 36 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

►**TTL (Page 65)**
►CMOS 3.5 series
►CMOS 5 Series
►Power dissipation of all circuits increases with time.

Question No: 37 (Marks: 1) - Please choose one

When the control line in tri-state buffer is high the buffer operates like a _____gate

►AND
►OR
►**NOT (Page 196)**
►XOR

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Question No: 38 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.
►Low switching speeds, high power dissipation
►Fast switching speeds, high power dissipation
►**Fast switching speeds, very low power dissipation (Page 61)**
►Low switching speeds, very low power dissipation

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one (Page 40)**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 2 (Marks: 1) - Please choose one
The OR Gate performs a Boolean _____ function

► **Addition (Page 42) rep**
► Subtraction
► Multiplication
► Division

Question No: 3 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

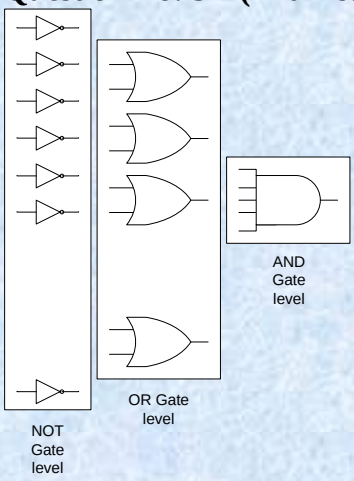
► **True rep Click here for Detail**
► False

Question No: 4 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► **A > B = 0, A < B = 1, A = B = 1**

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Question No: 5 (Marks: 1) - Please choose one

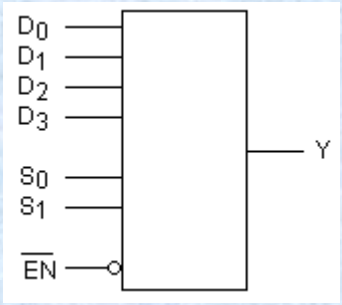


The diagram above shows the general implementation of _____ form

- ► boolean
- ► arbitrary
- ► **POS (Page 122)**
- ► SOP

Question No: 6 (Marks: 1) - Please choose one

The device shown here is most likely a



- ► Comparator
- ► **Multiplexer** **Click here for detail**
- ► Demultiplexer
- ► Parity generator

Question No: 7 (Marks: 1) - Please choose one

Demultiplexer converts _____ data to _____ data

- ► Parallel data, serial data
- ► **Serial data, parallel data (Page 356)**
- ► Encoded data, decoded data
- ► All of the given options.

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Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____
- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228) rep**
- ► Bi-stable singlevibrators

Question No: 9 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
- ► 0
- ► **1 (Page 230)**
- ► Invalid
- ► Input is invalid

Question No: 10 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
- ► 0
- ► 1
- ► **Invalid (Page 230)**
- ► Input is invalid

Question No: 11 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 12 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 13 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

- ► Using S-R Flop-Flop
- ► D-flipflop
- ► **J-K flip-flop (Page 252)**
- ► T-Flip-Flop

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Question No: 14 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

- ► True
- ► **False (Page 245)**

Question No: 15 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 16 (Marks: 1) - Please choose one
A negative edge-triggered flip-flop changes its state **when** _____

- ► Enable input (EN) is set
- ► Preset input (PRE) is set
- ► Low-to-high transition of clock
- ► **High-to-low transition of clock (Page 228)**

Question No: 17 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

- ► 10 mW
- ► **25 mW (Page 242)**
- ► 64 mW
- ► 1024

Question No: 18 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- ► Race condition
- ► **Clock Skew (Page 226) rep**
- ► Ripple Effect
- ► None of given options

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

- ► 3
- ► 7
- ► **8 (Page 272) rep**
- ► 15

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Question No: 20 (Marks: 1) - Please choose one
A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

- ► 10 Hz
- ► **50 Hz (Page 298)**
- ► 100 Hz
- ► 500 Hz

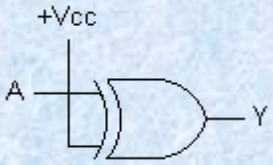
Question No: 21 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319)**

Question No: 22 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

- ► 3
- ► **4 (Page 281) rep**
- ► 7
- ► 10

Question No: 23 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for Detail rep**
- ► $\overline{A}$

Question No: 24 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

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Question No: 25 (Marks: 1) - Please choose one

In _____ the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

- ► Moore machine
- ► Mealy machine
- ► **Johnson counter (Page 354)**
- ► Ring counter

Question No: 26 (Marks: 1) - Please choose one

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

- ► Moore machine
- ► Mealy machine
- ► Johnson counter
- ► **Ring counter (Page 355) rep**

Question No: 27 (Marks: 1) - Please choose one

Which is not characteristic of a shift register?

- ► **Serial in/parallel in (Page 346)**
- ► Serial in/parallel out
- ► Parallel in/serial out
- ► Parallel in/parallel out

Question No: 28 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► **1100**
- ► 0011
- ► **0000 Click here for detail rep**
- ► 1111

Question No: 29 (Marks: 1) - Please choose one

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

- ► Write Time
- ► Recycle Time
- ► Refresh Time
- ► **Access Time (Page 417) rep**

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Question No: 30 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354) rep**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

- ► FALSE
- ► **TRUE (Page 250)**

Question No: 2 (Marks: 1) - Please choose one
The output of an XNOR gate is 1 when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

- ► I Only
- ► IV Only
- ► I and IV only
- ► **II and III only (Page 53)**

Question No: 3 (Marks: 1) - Please choose one
NAND gate is formed by connecting _____

- ► **AND Gate and then NOT Gate (Page 45)**
- ► NOT Gate and then AND Gate
- ► AND Gate and then OR Gate
- ► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

- ► Zero
- ► **One (Page 46)**
- ► Undefined
- ► No output as input is invalid

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Question No: 5 (Marks: 1) - Please choose one
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

- ► Radiation-Erase programming method (REPM)
- ► **In-System Programming (ISP) (Page 194)**
- ► In-chip Programming (ICP)
- ► Electronically-Erase programming method(EEPM)

Question No: 6 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

- ► !
- ► &
- ► **# (Page 201) rep**
- ► $

Question No: 7 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

- ► 0
- ► 1
- ► **Invalid (Page 230) rep**
- ► Input is invalid

Question No: 8 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 9 (Marks: 1) - Please choose one
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

- ► 0
- ► **1 (Page 227) rep**
- ► Q(t)
- ► Invalid

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

- ► True
- ► **False (Page 245) rep**

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Question No: 11 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

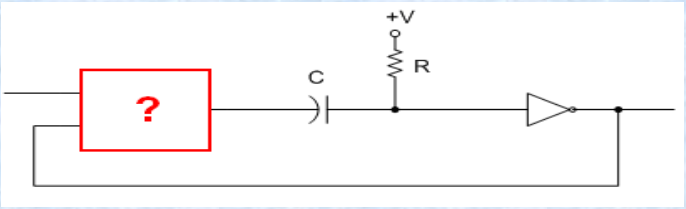
Question No: 12 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

- ► J-K input
- ► S-R input
- ► D input
- ► **Clear Input (CLR) (Page 235) rep**

Question No: 13 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 14 (Marks: 1) - Please choose one
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



- ► AND
- ► NAND
- ► NOR
- ► **XNOR (Page 262)**

Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the combination of current state and inputs.

- ► **Mealy machine (Page 332)**
- ► Moore Machine
- ► State Reduction table
- ► State Assignment table

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Question No: 16 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335) rep**

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► **Parallel data to serial (Page 356) rep**
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 19 (Marks: 1) - Please choose one
In the following statement
Z PIN 20 ISTYPE 'reg.invert';
The keyword "reg.invert" indicates _____

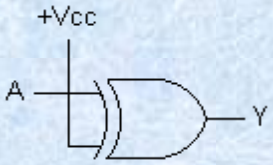
- ► An inverted register input
- ► An inverted register input at pin 20
- ► Active-high Registered Mode output
- ► **Active-low Registered Mode output (Page 360)**

Question No: 20 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

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Question No: 21 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for detail rep**
- ► $\overline{A}$

Question No: 22 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

Question No: 23 (Marks: 1) - Please choose one
A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/$\overline{\text{LEFT}}$ input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

- ► 1110
- ► 0111
- ► 1000
- ► **1001 Click he re for detail**

Question No: 24 (Marks: 1) - Please choose one
The high density FLASH memory cell is implemented using _____

- ► **1 floating-gate MOS transistor (Page 419) rep**
- ► 2 floating-gate MOS transistors
- ► 4 floating-gate MOS transistors
- ► 6 floating-gate MOS transistors

Question No: 25 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

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Question No: 26 (Marks: 1) - Please choose one

If the FIFO Memory output is already filled with data then _____

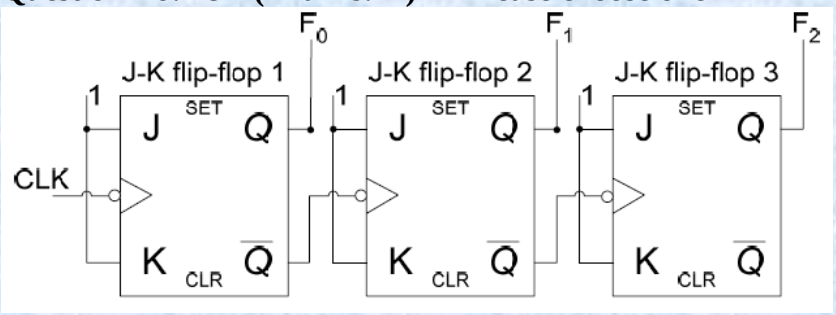
- ► It is locked; no data is allowed to enter
- ► It is not locked; the new data overwrites the previous data.
- ► Previous data is swapped out of memory and new data enters
- ► **None of given options**

Question No: 27 (Marks: 1) - Please choose one

The process of converting the analogue signal into a digital representation (code) is known as _____

- ► Strobing
- ► Amplification
- ► **Quantization (Page 445)**
- ► Digitization

Question No: 28 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270) rep**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 29 (Marks: 1) - Please choose one

$(A + B)(A + \overline{B} + C)(\overline{A} + C)$ is an example of _____

- ► **Product of sum form (Page 77)**
- ► Sum of product form
- ► Demorgans law
- ► Associative law

Question No: 30 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

- ► Q2:= Q1 $ X $ Q3
- ► **Q2:= Q1 # X # Q3 (Page 210)**
- ► Q2:= Q1 & X & Q3
- ► Q2:= Q1 ! X ! Q3

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FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
Caveman number system is Base _____ number system

► 2
► **5 (Page 11)**
► 10
► 16

Question No: 2 (Marks: 1) - Please choose one
The output of an XOR gate is zero (0) when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 3 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____**10001(right opt is not given)**

► 11101
► 11011
► **10111 (According to rule) rep**
► 11110

Question No: 4 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True Click here for Detail rep**
► False

Question No: 5 (Marks: 1) - Please choose one
The simplest and most commonly used Decoders are the _____ Decoders
► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

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Question No: 6 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 7 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

► **True (Page 161)**
► False

Question No: 8 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 9 (Marks: 1) - Please choose one
If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245) rep**

Question No: 11 (Marks: 1) - Please choose one
The low to high or high to low transition of the clock is considered to be a(n) _____

► State
► **Edge (Page 228)**
► Trigger
► One-shot

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Question No: 12 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 13 (Marks: 1) - Please choose one
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 14 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
► Ten
► Eight
► Three
► **Two (Page 262) rep**

Question No: 15 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 255) rep**

Question No: 16 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 17 (Marks: 1) - Please choose one
A transparent mode means _____

► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

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Question No: 18 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 19 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356) rep**
► Serial in / Parallel out shift register
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 20 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356) rep**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 21 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 22 (Marks: 1) - Please choose one
Smallest unit of binary data is a _____

► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 23 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394) rep**
► 8
► 16

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Question No: 24 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183) rep**

Question No: 25 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 27 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424) rep**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 28 (Marks: 1) - Please choose one **(Diagram is missing)**
In the circuit diagram of 3-bit synchronous counter shown above, The red rectangle would be replaced by which gate?
► **AND**
► OR
► NAND
► XNOR

Question No: 29 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2n (2 raise to power n)
► n2 (n raise to power 2)

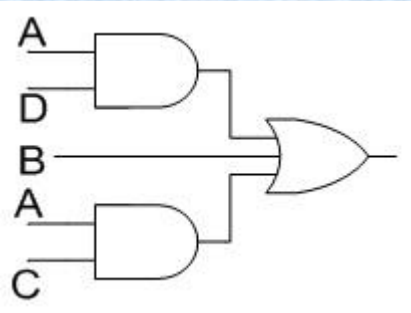
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Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78) rep**

Question No: 2 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "+7"

► **0000 (Page 34) rep**
► 1001
► 1000
► 1111

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Question No: 3 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

► = 0, Cout = 0
► **= 0, Cout = 1 (Page 135) rep**
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 5 (Marks: 1) - Please choose one
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 6 (Marks: 1) - Please choose one
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 7 (Marks: 1) - Please choose one
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.

► **TRUE (Page 182)**
► FALSE

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____

► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

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Question No: 9 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 10 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 11 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

- ► GATED FLIP-FLOPS
- ► PULSE TRIGGERED FLIP-FLOPS
- ► POSITIVE-EDGE TRIGGERED FLIP-FLOPS
- ► **NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267) rep**

Question No: 12 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319) rep**

Question No: 13 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____

- ► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
- ► MOD-10 AND MOD-6 COUNTERS
- ► MOD-10 AND MOD-2 COUNTERS
- ► **A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299) rep**

Question No: 14 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____

- ► **The next state of a given present state (Page 371) rep**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

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Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.

► Mealy machine
► **Moore Machine (Page 332) rep**
► State Reduction table
► State Assignment table

Question No: 16 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►**Parallel in / Serial out shift register (Page 356)**
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 19 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

► 2
► 4
► 6
► **8 (not sure) rep**

Question No: 20 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.
► 1
► 2
► 4
► **8 (Page 356)**

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Question No: 21 (Marks: 1) - Please choose one
5-BIT JOHNSON COUNTER SEQUENCES THROUGH ____ STATES

► 7
► **10 (Page 354) rep**
► 32
► 25

Question No: 22 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►**Ring counter (Page 355)**

Question No: 23 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 24 (Marks: 1) - Please choose one
If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 25 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 26 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.
► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

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Question No: 27 (Marks: 1) - Please choose one **(Diagram is missing)**

In the circuit diagram of 3-bit synchronous counterThe red rectangle, shown above would be replaced which gate?

► AND
► OR
► NAND
► XNOR

Question No: 28 (Marks: 1) - Please choose one

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------

► THE FLOP-FLOP IS TRIGGERED
► Q=0 AND Q'=1
► Q=1 AND Q'=0
► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)**

Question No: 29 (Marks: 1) - Please choose one

A frequency counter _____

► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301) rep**
► Counts high and low range of given clock pulse
► None of given options

Question No: 30 (Marks: 1) - Please choose one

Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

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CS302 Digital Logic Design Solved MCQs Final Term (AIO)

Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356)**

Question No: 2 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► **Current state and external input (Page 318)**
- ► Input and clock signal applied

Question No: 3 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 299)**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 4 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221)**
- ► False

Question No: 5 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 6 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

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Question No: 7 (Marks: 1) - Please choose one
_____ is said to occur when multiple internal variables change due to change in one input variable

► Clock Skew
► **Race condition (Page 267)**
► Hold delay
► Hold and Wait

Question No: 8 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

► **Asynchronous, synchronous (Page 369)**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 9 (Marks: 1) - Please choose one
A decade counter is _____.
► Mod-3 counter
► Mod-5 counter
► Mod-8 counter
► **Mod-10 counter (Page 274)**

Question No: 10 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356)**
► Remains in previous state
► State of transmission line is not used to start transmission



Question No: 11 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 12 (Marks: 1) - Please choose one
The output of this circuit is always _____.
► 1
► 0
► **A**
►

Question No: 13 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"
► 1110
► 1100
► 1000
► **0000 (Page 34)**

Question No: 14 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

► **Vout / Vin = - Rf / Ri (Page 446)**
► Vout / Rf = - Vin / Ri
► Rf / Vin = - Ri / Vout
► Rf / Vin = Ri / Vout

Question No: 15 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439)**

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► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 16 (Marks: 1) - Please choose one
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

Question No: 17 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____
► The organization of memory
► The structure of memory
► The size of decoding unit
► **The size of the address bus of the microprocessor (Page 430)**

Question No: 18 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429)**
► Flash Memory
► Bust Flash Memory

Question No: 19 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

► 213
► 123
► **127**
► 345



Question No: 20 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.
► **J-K input (Page 235)**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 21 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226)**
► Ripple Effect
► None of given options

Question No: 22 (Marks: 1) - Please choose one
Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101 (not sure)**
► 1011
► 1111

Question No: 23 (Marks: 1) - Please choose one
In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 332)**
► Current state and outputs

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► Previous state and inputs
► Previous state and outputs

Question No: 24 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

► State diagram
► Next state table
► State reduction
► **State assignment (Page 335)**

Question No: 25 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
► 1100
► 0011
► **0000** Click here for detail
► 1111

Question No: 27 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options



. **Question No: 28 (Marks: 1) - Please choose one**
The diagram given below represents _____
► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

Question No: 29 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 30 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 31 (Marks: 1) - Please choose one
A GAL is essentially a _____.

► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

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Question No: 32 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

► Sequential Access
► MOS Access
► **FAST Mode Page Access (Page 413)**
► None of given options

Question No: 33 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 34 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

FINALTERM EXAMINATION
Spring 2010



Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to
shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 2 (Marks: 1) - Please choose one
A frequency counter _____

► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301)**
► Counts high and low range of given clock pulse
► None of given options

Question No: 3 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

► State variable, current state
► Current state, flip-flop output
► Current state and external input
► **Input and clock signal applied (Page 305)**

Question No: 4 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 229) rep**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► **True (Page 221) rep**
► False

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Question No: 6 (Marks: 1) - Please choose one
Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228)**
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242) rep**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 9 (Marks: 1) - Please choose one
_____ is said to occur when multiple internal variables change due to change in one input variable



- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 10 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____

- ► **The next state of a given present state (Page 371)**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one
A logic circuit with an output

consists of _____.

- ► two AND gates, two OR gates, two inverters
- ► three AND gates, two OR gates, one inverter
- ► **two AND gates, one OR gate, two inverters (Lecture 8)**
- ► two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one
A decade counter is _____.

- ► Mod-3 counter

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► Mod-5 counter
► Mod-8 counter
► **Mod-10 counter (Page 274)**

Question No: 14 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 15 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.
► 1
► 0
► **A** Click here for detail **rep**
►

Question No: 17 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

► 1110
► 1100
► 1000
► **0000 (Page 34) rep**



Question No: 18 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

► **$V_{out} / V_{in} = - R_f / Ri$ (Page 446)**
► Vout / Rf = - Vin / Ri
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / Vout$

Question No: 19 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 20 (Marks: 1) - Please choose one
DRAM stands for _____

► **Dynamic RAM (Page 407)**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 21 (Marks: 1) - Please choose one
The three fundamental gates are _____

► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

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Question No: 22 (Marks: 1) - Please choose one
Which of the following statement is true regarding above block diagram?

- ► Triggering takes place on the negative-going edge of the CLK pulse
- ► Triggering takes place on the positive-going edge of the CLK pulse
- ► Triggering can take place anytime during the HIGH level of the CLK waveform
- ► Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- ► The organization of memory
- ► The structure of memory
- ► The size of decoding unit
- ► **The size of the address bus of the microprocessor (Page 430) rep**

Question No: 24 (Marks: 1) - Please choose one
The expression F=A+B+C describes the operation of three bits _____ Gate.

- ► **OR (Page 42)**
- ► AND
- ► NOT
- ► NAND

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for_____

- ► FIFO memory
- ► **LIFO memory (Page 429) rep**
- ► Flash Memory
- ► Bust Flash Memory



Question No: 26 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

- ► 213
- ► 123
- ► **127**
- ► 345

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

- ► 8-bit
- ► 16-bit
- ► **32-bit (Page 25)**
- ► 64-bit

Question No: 2 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____

- ► 11101
- ► 11011
- ► **10111 (According to rule)**
- ► 11110

Question No: 3 (Marks: 1) - Please choose one
The basic building block for a logical circuit is _____

- ► A Flip-Flop
- ► **A Logical Gate (Page 7)**
- ► An Adder
- ► None of given options

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Question No: 4 (Marks: 1) - Please choose one
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

► Undefined
► One
► **Zero (According to rule)**
► No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map
► 2
► 8
► **12 (According to rule "2^n")**
► 16

Question No: 6 (Marks: 1) - Please choose one
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 7 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

► **J-K input (Page 235) rep**
► EN input
► Preset input (PRE)
► Clear Input (CLR)



Question No: 8 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 235)**

Question No: 9 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

► **Asynchronous, synchronous (Page 369) rep**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 11 (Marks: 1) - Please choose one
Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101 (not sure)**
► 1011
► 1111

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Question No: 12 (Marks: 1) - Please choose one
In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one
_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

Question No: 14 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

► State diagram
► Next state table
► State reduction
► **State assignment (Page 335)**

Question No: 15 (Marks: 1) - Please choose one
The best state assignment tends to _____.

► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
► Minimizes the number of state variables that don‟t change in a group of related states
► Minimize the equivalent states
► None of given options



Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.
► 1
► 0
► **A** Click here for detail **rep**
►

Question No: 17 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 18 (Marks: 1) - Please choose one
5-bit Johnson counter sequences through ____ states

► 7
► **10 (Page 354)**
► 32
► 25

Question No: 19 (Marks: 1) - Please choose one
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

► 1100
► 0011

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► **0000** Click here for detail **rep**
► 1111

Question No: 20 (Marks: 1) - Please choose one
The address from which the data is read, is provided by _____

► Depends on circuitry
► None of given options
► RAM
► **Microprocessor (Page 397)**

Question No: 21 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424)**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 22 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options



Question No: 23 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

► **Vout / Vin = - R_f / Ri (Page 446)**
► Vout / Rf = - V_{in} / R_i
► R_f / V_{in} = - R_i / V_{out}
► Rf / Vin = Ri / Vout

Question No: 24 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

Question No: 25 (Marks: 1) - Please choose one
Above is the circuit diagram of _____.

► **Asynchronous up-counter (Page 270)**
► Asynchronous down-counter
► Synchronous up-counter
► Synchronous down-counter

Question No: 26 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is
► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354)**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

FINALTERM EXAMINATION
Spring 2010

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Question No: 1 (Marks: 1) - Please choose one
"A + B = B + A" is _____

- ► Demorgan‟s Law
- ► Distributive Law
- ► **Commutative Law (Page 72)**
- ► Associative Law

Question No: 2 (Marks: 1) - Please choose one
The diagram given below represents _____

- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► **Sum of product form (Page 78) rep**

Question No: 3 (Marks: 1) - Please choose one
Following is standard POS expression

- ► **True (Lecture 9)**
- ► False

Question No: 4 (Marks: 1) - Please choose one
An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

- ► Using a single comparator
- ► **Using Iterative Circuit based Comparators (Page 155)**
- ► Connecting comparators in vertical hierarchy
- ► Extra logic gates are always required.



Question No: 5 (Marks: 1) - Please choose one
Demultiplexer is also called

- ► Data selector
- ► Data router
- ► **Data distributor (Page 178)**
- ► Data encoder

Question No: 6 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 7 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 8 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

- ► 10 mW
- ► **25 mW (Page 242)**
- ► 64 mW
- ► 1024

Question No: 9 (Marks: 1) - Please choose one

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_____ counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**
► Synchronous
► Positive-Edge triggered
► Negative-Edge triggered

Question No: 10 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

► **ENP, ENT (Page 285) rep**
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 11 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Question No: 12 (Marks: 1) - Please choose one
In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs



Question No: 13 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

► 3
► **4 (Page 281)**
► 7
► 10

Question No: 14 (Marks: 1) - Please choose one
_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341) rep**
► State reduction
► Next state table
► State diagram

Question No: 15 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 16 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 17 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL

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► PAL that is programmed only by the manufacturer
► Very large PAL
►**Reprogrammable PAL (Page 183) rep**

Question No: 18 (Marks: 1) - Please choose one
The output of this circuit is always _____.
► 1
► 0
► **A** Click here For detail **rep**
►

Question No: 20 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

► Sequential Access
► MOS Access
► **FAST Mode Page Access (Page 413) rep**
► None of given options

Question No: 21 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424) rep**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 22 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

► Read Only Memory
► **Fist In First Out Memory (Page 425) rep**
► Flash Memory
► Fast Page Access Mode Memory



Question No: 23 (Marks: 1) - Please choose one
A frequency counter _____

► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301) rep**
► Counts high and low range of given clock pulse
► None of given options

Question No: 24 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
The 4-bit 2"s complement representation of "+5" is _____

► 1010
► 1110

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► 1011
► **0101 (Page 22)**

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
The storage cell in SRAM is
a flip –flop ►
►**a capacitor (Page 407)**
a fuse ►
a magnetic domain ►

Question No: 2 (Marks: 1) - Please choose one
What is the difference between a D latch and a D flip-flop?

The D latch has a clock input. ►
The D flip-flop has an enable input. ►
The D latch is used for faster operation. ►
►**The D flip-flop has a clock input.** Click here for detail

Question No: 3 (Marks: 1) - Please choose one
For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH.

►**toggle** Click here for detail
set ►
reset ►
not change ►



Question No: 4 (Marks: 1) - Please choose one
The OR gate performs Boolean _____.

multiplication ►
subtraction ►
division ►
►**addition (Page 42)**

Question No: 5 (Marks: 1) - Please choose one
If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

► **set (Page 219)**
► reset
► invalid
► clear

5. Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.

A = 1, B = 0, C = 0, D = 0 ►
►**A = 1, B = 0, C = 1, D = 0 (Lecture 8)**
A = 0, B = 1, C = 0, D = 0 ►
►A = 1, B = 0, C = 1, D = 1

Question No: 6 (Marks: 1) - Please choose one
The power dissipation, *P*D, of a logic gate is the product of the

►**dc supply voltage and the peak current** Click here for detail
►dc supply voltage and the average supply current
►ac supply voltage and the peak current
►ac supply voltage and the average supply current

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Question No: 7 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

►**True** Click here for detail
►False

Question No: 8 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

►**True (Page 50)**
►False

Question No: 9 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

►**A parallel to serial converter circuit (Page 244)**
►A counter circuit
►A BCD to Decimal decoder
►A 2-to-8 bit decoder

Question No: 10 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

►4
►**8 (Page 89)**
►12
►16



Question No: 11 (Marks: 1) - Please choose one
In designing any counter the transition from a current state to the next sate is determined by

►**Current state and inputs (Page 332)**
►Only inputs
►Only current state
►current state and outputs

Question No: 12 (Marks: 1) - Please choose one
Sum term (Max term) is implemented using _____ gates

►**OR (Page 78)**
►AND
►NOT
►OR-AND

Question No: 13 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____

► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 14 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

►2
►4
►6
►**8 (not sure)**

Question No: 15 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO

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_____

►THE FLOP-FLOP IS TRIGGERED
►Q=0 AND Q‟=1
►Q=1 AND Q'=0 (Page 233)
►THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

Question No: 16 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

►0
►1 (Page 230)
►Invalid
►Input is invalid

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
► 0
► 1
► Invalid (Page 233)
► Input is invalid

Question No: 17 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

►Set-up time
►Hold time (Page 242) rep
►Pulse Interval time
►Pulse Stability time (PST)



Question No: 18 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by
_____

►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

►3
►7
►8 (Page 272)
►15

Question No: 20 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 21 (Marks: 1) - Please choose one
The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

►Write Time

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►Recycle Time
►Refresh Time
►**Access Time (Page 417)**

Question No: 22 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

►Ten
►Eight
►Three
►**Two (Page 262)**

Question No: 23 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

►Race condition
►**Clock Skew (Page 226) rep**
►Ripple Effect
►None of given options

Question No: 24 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

►**Parallel in / Serial out shift register (Page 356)**
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register



Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

= 0, Cout = 0 ►
►**= 0, Cout = 1 (Page 135)**
= 1, Cout = 0 ►
= 1, Cout = 1 ►

Question No: 27 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

►GATED FLIP-FLOPS
►PULSE TRIGGERED FLIP-FLOPS
►POSITIVE-EDGE TRIGGERED FLIP-FLOPS
►**NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)**

Question No: 28 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 29 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____

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►ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
►MOD-10 AND MOD-6 COUNTERS
►MOD-10 AND MOD-2 COUNTERS
►**A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)**

Question No: 30 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____

► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 31 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 32 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code



Question No: 33 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

►State diagram
►**Next state table**
►State reduction
►**State assignment (Page 335) rep**

Question No: 34 (Marks: 1) - Please choose one
The high density FLASH memory cell is implemented using _____

►**1 floating-gate MOS transistor (Page 419)**
►2 floating-gate MOS transistors
►4 floating-gate MOS transistors
►6 floating-gate MOS transistors

Question No: 35 (Marks: 1) - Please choose one
Q2 :=Q1 OR X OR Q3
The above ABEL expression will be

►Q2:= Q1 $ X $ Q3
►**Q2:= Q1 # X # Q3 (Page 210)**
►Q2:= Q1 & X & Q3
►Q2:= Q1 ! X ! Q3

Question No: 36 (Marks: 1) - Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

►**TTL (Page 65)**
►CMOS 3.5 series
►CMOS 5 Series
►Power dissipation of all circuits increases with time.

Question No: 37 (Marks: 1) - Please choose one

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When the control line in tri-state buffer is high the buffer operates like a _____gate

►AND
►OR
►**NOT (Page 196)**
►XOR

Question No: 38 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

►Low switching speeds, high power dissipation
►Fast switching speeds, high power dissipation
►**Fast switching speeds, very low power dissipation (Page 61)**
►Low switching speeds, very low power dissipation

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one (Page 40)**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 2 (Marks: 1) - Please choose one
The OR Gate performs a Boolean _____ function

► **Addition (Page 42) rep**
► Subtraction
► Multiplication
► Division



Question No: 3 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the
resulting output of each value.

► **True rep** Click here for Detail
► False

Question No: 4 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► **A > B = 0, A < B = 1, A = B = 1**

The diagram above shows the general implementation of _____ form

► boolean
► arbitrary
► **POS (Page 122)**
► SOP

Question No: 6 (Marks: 1) - Please choose one
The device shown here is most likely a
► Comparator

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► **Multiplexer** Click here for detail
► Demultiplexer
► Parity generator

Question No: 7 (Marks: 1) - Please choose one
Demultiplexer converts _____ data to _____ data

► Parallel data, serial data
► **Serial data, parallel data (Page 356)**
► Encoded data, decoded data
► All of the given options.

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____

► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228) rep**
► Bi-stable singlevibrators

Question No: 9 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid



Question No: 10 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

► 0
► 1
► **Invalid (Page 230)**
► Input is invalid

Question No: 11 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► **Doesn't have an invalid state (Page 232) rep**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 12 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

► Set-up time
► **Hold time (Page 242)**
► Pulse Interval time
► Pulse Stability time (PST)

Question No: 13 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

► Using S-R Flop-Flop
► D-flipflop
► **J-K flip-flop (Page 252)**
► T-Flip-Flop

Question No: 14 (Marks: 1) - Please choose one

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In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245)**

Question No: 15 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228) rep**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 16 (Marks: 1) - Please choose one
A negative edge-triggered flip-flop changes its state **when** _____

► Enable input (EN) is set
► Preset input (PRE) is set
► Low-to-high transition of clock
► **High-to-low transition of clock (Page 228)**

Question No: 17 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024



Question No: 18 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to
propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

► 3
► 7
► **8 (Page 272) rep**
► 15

Question No: 20 (Marks: 1) - Please choose one
A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

► 10 Hz
► **50 Hz (Page 298)**
► 100 Hz
► 500 Hz

Question No: 21 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► **state diagram (Page 319)**

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Question No: 22 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

- ► 3
- ► **4 (Page 281) rep**
- ► 7
- ► 10

Question No: 23 (Marks: 1) - Please choose one
The output of this circuit is always _____.

- ► 1
- ► 0
- ► **A Click here for Detail rep**
- ►

Question No: 24 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

Question No: 25 (Marks: 1) - Please choose one
In _____ the ^{Q} output of the last flip-flop of the shift register is connected to the data input of the first flip-
flop.



- ► Moore machine
- ► Mealy machine
- ► **Johnson counter (Page 354)**
- ► Ring counter

Question No: 26 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop
of the shift register.

- ► Moore machine
- ► Mealy machine
- ► Johnson counter
- ► **Ring counter (Page 355) rep**

Question No: 27 (Marks: 1) - Please choose one
Which is not characteristic of a shift register?

- ► **Serial in/parallel in (Page 346)**
- ► Serial in/parallel out
- ► Parallel in/serial out
- ► Parallel in/parallel out

Question No: 28 (Marks: 1) - Please choose one
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► **1100**
- ► 0011
- ► **0000 Click here for detail rep**
- ► 1111

Question No: 29 (Marks: 1) - Please choose one
The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

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► Write Time
► Recycle Time
► Refresh Time
► **Access Time (Page 417) rep**

Question No: 30 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

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Question No: 1 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► FALSE
► **TRUE (Page 250)**

Question No: 2 (Marks: 1) - Please choose one
The output of an XNOR gate is 1 when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one
► I Only
► IV Only
► I and IV only
► **II and III only (Page 53)**



Question No: 3 (Marks: 1) - Please choose one
NAND gate is formed by connecting _____

► **AND Gate and then NOT Gate (Page 45)**
► NOT Gate and then AND Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

► Zero
► **One (Page 46)**
► Undefined
► No output as input is invalid

Question No: 5 (Marks: 1) - Please choose one
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

► Radiation-Erase programming method (REPM)
► **In-System Programming (ISP) (Page 194)**
► In-chip Programming (ICP)
► Electronically-Erase programming method(EEPM)

Question No: 6 (Marks: 1) - Please choose one
The ABEL symbol for “OR” operation is

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► !
► &
► **# (Page 201) rep**
► $

Question No: 7 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
► 0
► 1
► **Invalid (Page 230) rep**
► Input is invalid

Question No: 8 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► **Doesn't have an invalid state (Page 232) rep**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 9 (Marks: 1) - Please choose one
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

► 0
► **1 (Page 227) rep**
► Q(t)
► Invalid



Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock
► True
► **False (Page 245) rep**

Question No: 11 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228) rep**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 12 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.
► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 235) rep**

Question No: 13 (Marks: 1) - Please choose one
The _____ input overrides the _____ input
► **Asynchronous, synchronous (Page 369) rep**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 14 (Marks: 1) - Please choose one
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.
► AND
► NAND
► NOR
► **XNOR (Page 262)**

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Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the combination of current state and inputs.

► **Mealy machine (Page 332)**
► Moore Machine
► State Reduction table
► State Assignment table

Question No: 16 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.
► State diagram
► Next state table
► State reduction
► **State assignment (Page 335) rep**

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission



Question No: 19 (Marks: 1) - Please choose one
In the following statement
Z PIN 20 ISTYPE „reg.invert";
The keyword "reg.invert" indicates _____

► An inverted register input
► An inverted register input at pin 20
► Active-high Registered Mode output
► **Active-low Registered Mode output (Page 360)**

Question No: 20 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 21 (Marks: 1) - Please choose one
The output of this circuit is always _____.
► 1
► 0
► **A Click here for detail rep**
►

Question No: 22 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

► 2
► 4
► 6
► **8 (not sure)**

Question No: 23 (Marks: 1) - Please choose one

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A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

- ► 1110
- ► 0111
- ► 1000
- ► **1001** **Click he re for detail**

Question No: 24 (Marks: 1) - Please choose one
The high density FLASH memory cell is implemented using _____

- ► **1 floating-gate MOS transistor (Page 419) rep**
- ► 2 floating-gate MOS transistors
- ► 4 floating-gate MOS transistors
- ► 6 floating-gate MOS transistors

Question No: 25 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 26 (Marks: 1) - Please choose one
If the FIFO Memory output is already filled with data then _____

- ► It is locked; no data is allowed to enter
- ► It is not locked; the new data overwrites the previous data.
- ► Previous data is swapped out of memory and new data enters
- ► **None of given options**



Question No: 27 (Marks: 1) - Please choose one
The process of converting the analogue signal into a digital representation (code) is known as _____

- ► Strobing
- ► Amplification
- ► **Quantization (Page 445)**
- ► Digitization

Question No: 28 (Marks: 1) - Please choose one
Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270) rep**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 29 (Marks: 1) - Please choose one
(A + B)(A + B + C)(A + C)
is an example of _____

- ► **Product of sum form (Page 77)**
- ► Sum of product form
- ► Demorgans law
- ► Associative law

Question No: 30 (Marks: 1) - Please choose one
Q2 :=Q1 OR X OR Q3
The above ABEL expression will be

- ► Q2:= Q1 $ X $ Q3
- ► **Q2:= Q1 # X # Q3 (Page 210)**
- ► Q2:= Q1 & X & Q3
- ► Q2:= Q1 ! X ! Q3

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Question No: 1 (Marks: 1) - Please choose one
Caveman number system is Base _____ number system

► 2
► **5 (Page 11)**
► 10
► 16

Question No: 2 (Marks: 1) - Please choose one
The output of an XOR gate is zero (0) when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 3 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____**10001(right opt is not given)**

► 11101
► 11011
► **10111 (According to rule) rep**
► 11110



Question No: 4 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the
resulting output of each value.

► **True** Click here for Detail **rep**
► False

Question No: 5 (Marks: 1) - Please choose one
The simplest and most commonly used Decoders are the _____ Decoders
► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

Question No: 6 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 7 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

► **True (Page 161)**
► False

Question No: 8 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

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Question No: 9 (Marks: 1) - Please choose one
If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245) rep**

Question No: 11 (Marks: 1) - Please choose one
The low to high or high to low transition of the clock is considered to be a(n) _____

► State
► **Edge (Page 228)**
► Trigger
► One-shot

Question No: 12 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set



Question No: 13 (Marks: 1) - Please choose one
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 14 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
► Ten
► Eight
► Three
► **Two (Page 262) rep**

Question No: 15 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 255) rep**

Question No: 16 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 17 (Marks: 1) - Please choose one
A transparent mode means _____

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► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

Question No: 18 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 19 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356) rep**
► Serial in / Parallel out shift register
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 20 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356) rep**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 21 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____



► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 22 (Marks: 1) - Please choose one
Smallest unit of binary data is a _____

► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 23 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394) rep**
► 8
► 16

Question No: 24 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183) rep**

Question No: 25 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

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Question No: 26 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 27 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424) rep**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 28 (Marks: 1) - Please choose one

(Diagram is missing)
In the circuit diagram of 3-bit synchronous counter shown above, The red rectangle would be replaced by which gate?
► **AND**
► OR
► NAND
► XNOR

Question No: 29 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is



► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2n (2 raise to power n)
► n2 (n raise to power 2)

Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

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Question No: 1 (Marks: 1) - Please choose one
The diagram given below represents _____
► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78) rep**

Question No: 2 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "+7"

► **0000 (Page 34) rep**
► 1001
► 1000
► 1111

Question No: 3 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate

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► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

= 0, Cout = 0 ►
►**= 0, Cout = 1 (Page 135) rep**
= 1, Cout = 0 ►
= 1, Cout = 1 ►

Question No: 5 (Marks: 1) - Please choose one
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 6 (Marks: 1) - Please choose one
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

► AND
► **OR (Page 171)**
► NAND
► XOR



Question No: 7 (Marks: 1) - Please choose one
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.

► **TRUE (Page 182)**
► FALSE

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____

► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

Question No: 9 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 10 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

► **J-K input (Page 235)**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 11 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

► GATED FLIP-FLOPS
► PULSE TRIGGERED FLIP-FLOPS
► POSITIVE-EDGE TRIGGERED FLIP-FLOPS
► **NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267) rep**

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Question No: 12 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► **state diagram (Page 319) rep**

Question No: 13 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____

► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
► MOD-10 AND MOD-6 COUNTERS
► MOD-10 AND MOD-2 COUNTERS
► **A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299) rep**

Question No: 14 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.

► Mealy machine
► **Moore Machine (Page 332) rep**
► State Reduction table
► State Assignment table



Question No: 16 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►**Parallel in / Serial out shift register (Page 356)**
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 19 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

► 2
► 4
► 6
► **8 (not sure) rep**

Question No: 20 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

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► 1
► 2
► 4
► **8 (Page 356)**

Question No: 21 (Marks: 1) - Please choose one
5-BIT JOHNSON COUNTER SEQUENCES THROUGH ____ STATES

► 7
► **10 (Page 354) rep**
► 32
► 25

Question No: 22 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►**Ring counter (Page 355)**

Question No: 23 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options



Question No: 24 (Marks: 1) - Please choose one
If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 25 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 26 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.
► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

Question No: 27 (Marks: 1) - Please choose one
In the circuit diagram of 3-bit synchronous counterThe red rectangle, shown above would be replaced which gate?

► AND
► OR
► NAND
► XNOR

Question No: 28 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------
__
► THE FLOP-FLOP IS TRIGGERED
► Q=0 AND Q‟=1
► Q=1 AND Q‟=0
► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)**

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Question No: 29 (Marks: 1) - Please choose one
A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301) rep**
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

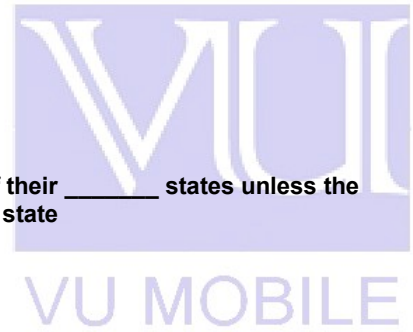
► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

The power consumed by a flip-flop is defined by _____
Select correct option:

P = Icc x Rcc
P = Vcc x Rcc
P = Vcc x Icc
P = Mcc x Vcc
3:31 PM 3rd na??

If S=1 and R=0, then for positive edge triggered flip-flop Q(t+1) = _____
Select correct option:

0
1
Invalid
Input is invalid





Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
Select correct option:

Ten
Eight
Three
Two

When the both inputs of edge-triggered J-K flop-flop are set to logic zero _____
Select correct option:

The flop-flop is triggered
Q=0 and Q'=1
Q=1 and Q'=0
The output of flip-flop remains unchanged

The counter states or the range of numbers of a counter is determined by the formula. "n" represents the total number of flip-flops)
Select correct option:

(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

If S=1 and R=1, for negative edge triggered flip-flop then Q(t+1) = _____
Select correct option:

0
1
Invalid

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Input is invalid

If the S and R inputs of the gated S-R latch are connected together using a ____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)
Select correct option:

AND
OR
NOT
XOR

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.
Select correct option:

Set-up time
Hold time
Pulse Interval time
Pulse Stability time (PST)

The Synchronous counters are also known as Ripple Counters:
Select correct option:

True
False

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
Select correct option:

10 mW
25 mW
64 mW
1024 mW



We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____
Select correct option:

Using S-R Flop-Flop
D-flipflop
J-K flip-flop
T-Flip-Flop
3:43 PM auhawan123: J-K flip-flop

If S=1 and R=1, for negative edge triggered flip-flop then Q(t+1) = _____
Select correct option:

0
1
Invalid
Input is invalid

A negative edge-triggered flip-flop changes its state when _____
Select correct option:

Enable input (EN) is set
Preset input (PRE) is set
Low-to-high transition of clock
High-to-low transition of clock

The terminal count of a 4-bit binary counter in the UP mode is_____
Select correct option:

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1100
0011
1111
0000

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)
Select correct option:
(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

PM RCO stands for _____
Select correct option:
Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter.it has.....parallel data inputs pins
Select correct option:

2
4
6
8



A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
Select correct option:

10 mW
25 mW
64 mW
1024 mW

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.
Select correct option:

Set-up time
Hold time
Pulse Interval time
Pulse Stability time (PST)

In Synchronous systems, the output of all the digital circuits changes when an enable signal is applied instead of the clock signal.
Select correct option:

True
False

If S=1 and R=0, then for positive edge triggered flip-flop Q(t+1) = _____
Select correct option:

0
1
Invalid
Input is invalid

In designing any synchronous counter a modulus number is used which determine the number of..... used in a counter
Select correct option:

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Registers
Flip Flops
Counters
Latches

A synchronous decade counter will have _____ flip-flops
Select correct option:

3
4
7
10

The terminal count of a 4-bit binary counter in the UP mode is_____
Select correct option:

1100
0011
1111
0000

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:

Race condition
Clock Skew
Ripple Effect
None of given options

A transparent mode means _____
Select correct option:

The changes in the data at the inputs of the latch are seen at the output
The changes in the data at the inputs of the latch are not seen at the output
Propagation Delay is zero (Output is immediately changed when clock signal is applied)
Input Hold time is zero (no need to maintain input after clock transition)



_____ Counters as the name indicates are not triggered simultaneously
Select correct option:

Asynchronous
Synchronous
Positive-Edge triggered
Negative-Edge triggered

In Master-Slave flip-flop setup, the master flip flop operates at _____
Select correct option:

Positive half cycle of pulse (Not sure)
Negative half cycle of pulse
Both Master-Slave operate simultaneously
Master-Slave flip-flop does not operate on pulses, rather it is edge triggered.

The power consumed by a flip-flop is defined by _____
Select correct option:

P = Icc x Rcc
P = Vcc x Rcc
P = Vcc x Icc
P = Mcc x Vcc

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A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
Select correct option:

10 mW
25 mW
64 mW
1024 mW

A one-shot mono-stable device contains _____
Select correct option:

AND gate, Resistor, Capacitor and NOT Gate
NAND gate, Resistor, Capacitor and NOT Gate (not sure)
NOR gate, Resistor, Capacitor and NOT Gate
XNOR gate, Resistor, Capacitor and NOT Gate

When the both inputs of edge-triggered J-K flop-flop are set to logic zero _____

Select correct option:

The flop-flop is triggered
Q=0 and Q'=1
Q=1 and Q'=0 (not sure)
The output of flip-flop remains unchanged

Flip flops are also called _____

Select correct option:

Bi-stable multivibrators
Bi-stable singlevibrators
Bi-stable dualvibrators
Bi-stable transformer

An Astable multivibrator is known as a(n) ____

Oscillator
Booster
One-shot
Dual-shot

A decade counter is _____

Mod-3 counter
Mod-5 counter
Mod-8 counter
Mod-10 counter

In Synchronous systems, the output of all the digital circuits changes when an enable signal is applied instead of the clock signal.

True
False (not sure)

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.

Set-up time
Hold time
Pulse Interval time
Pulse Stability time (PST)

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A mono-stable device only has a single stable state

Select correct option:

True
False

RCO stands for _____

Select correct option:

Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

A mono-stable device only has a single stable state

Select correct option:

True
False

The 74HC163 is a 4-bit Synchronous Counter.it has.....parallel data inputs pins

Select correct option:

2
4
6
8

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The Synchronous counters are also known as Ripple Counters:
Select correct option:

True
False

_____ Counters as the name indicates are not triggered simultaneously
Select correct option:

Asynchronous
Synchronous
Positive-Edge triggered
Negative-Edge triggered

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____
Select correct option:

111
110
010
none of given options

The terminal count of a 4-bit binary counter in the DOWN mode is_____
0000
0011
1100
1111

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

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Select correct option:

True
False

RCO stands for _____

Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

Select correct option:

True
False

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

Select correct option:

True
False

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

Select correct option:

True
False

For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

Select correct option:

0
1
Q(t)
Invalid

A flip-flop is presently in SET stae and must remain SET on the next cliock pulse. What must j and K be?

Select correct option:

J = 1, K = 0
J = 1, K = X(Don't care)
J = X(Don't care), K = 0
J = 0, K = X(Don't care)

Divide-by-160 counter is acheived by using

Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
DIV 16 and DIV 32 **(not sure)**
DIV 16 and DIV 10

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Three cascaded modulus-10 counters have an overall modulus of

Select correct option:

30
100

1000
0000

A standard SOP form has _____ terms that have all the variables in the domain of the expression.

And
OR
Sum
Not

Which one of the following is not a valid rule of Boolean algebra?

(a) A + 1 = 1
(b) A = Ā
(c) A.A = A
(d) A + 0 = A

How many data select lines are required for selecting eight inputs?
1
2
3 (correct)
4

If two adjacent 1s are detected in the input, the output is set to high. inp ut combinations will be

1) 0011
2) 0101
3) 1100
4) 1010

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The 4-variable Karnaugh Map (K-Map) has _____rows and ____colums

2,2
4,4,
4,2
2,4

The boolean expression A + B' + C is

a sum term
a literal term
a product term
a complemented term

The boolean expression AB'CD' is

a sum term
a product term
a literal term
always 1

Don't care conditions are marked as _____ in the output column of the function table

0
1

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X
None of the given options

An example of SOP expression is

A + B(C + D)
A'B + AC' + AB'C
(A' + B + C)(A + B' + C)
both (a) nad (b)

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

0
1
X (don't care condition)

Question # 1 of 10 (Start time: 03:15:33 PM) Total Marks: 1
The complement of a variable is always
Select correct option:

0
1
equal to the variable
the inverse of the variable

Question # 2 of 10 (Start time: 03:16:20 PM) Total Marks: 1
The 4-variable K-Map has _____ rows and _____ columns of cells.
Select correct option:

2, 2
2, 4
4, 2
4, 4

Question # 3 of 10 (Start time: 03:17:15 PM) Total Marks: 1
Half-Adder Logic circuit contains ___ XOR Gates.

0
2
4
6

Question # 4 of 10 (Start time: 03:18:46 PM) Total Marks: 1
The boolean expression X = AB + CD represents

two ORs ANDed together
a 4-input AND gate
two ANDs ORed together
an exclusive-Or

Question # 5 of 10 (Start time: 03:19:54 PM) Total Marks: 1
An example of SOP expression is

A + B(C + D)
A'B + AC' + AB'C
(A' + B + C)(A + B' + C)
both (a) nad (b)

Question # 6 of 10 (Start time: 03:21:10 PM) Total Marks: 1
Sum term (Max term) is implemented using _____ gates

OR
AND
NOT

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OR-AND

Question # 7 of 10 (Start time: 03:21:48 PM) Total Marks: 1
The domain of the expression AB'CD + AB' + C'D + B is

A and D
B only
A,B,C and D
none of these

Question # 8 of 10 (Start time: 03:22:52 PM) Total Marks: 1
A SOP expression having a domain of 3 variables will have a truth table having __ combinations of inputs and corresponding output values.

2
4
8
16

Question # 9 of 10 (Start time: 03:23:34 PM) Total Marks: 1
The boolean expression (A +C)(AB' +AC)(A'C' + B')can be simplified to
Select correct option:
AB'
AB + A'C
A'B + BC
AB + BC

Question # 10 of 10 (Start time: 03:24:48 PM) Total Marks: 1
The bolean expression A + BC equals

(A' + B)(A' + C)
(A + B)(A + C)
(A + B)(A' + C)
none of the above



Question # 4 of 10
If a circuit suffers "Clock Skew " problem, the output of circuit can't be guarantied.

True
False

Question # 5 of 10
A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____

0001
1111
1000
1110

Question # 6 of 10
Karnaugh map is used in designing

a clock
a counter
an UP/DOWN counter
All of the above

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Question # 8 of 10
Asynchronous mean that_____

Each flip-flop after the first one is enabled by the output of the preceding flip-flop
Each flip-flop is enabled by the output of the preceding flip-flop
Each flip-flop except the last one is enabled by the output of the preceding flip-flop
Each alternative flip-flop after the first one is enabled by the output of the preceding flip-flop

Question # 10 of 10
A modulus-14 counter has fourteen states requiring_____

14 Flip Flops
14 Registers
4 Flip Flops
4 Registers

X

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